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Mullard Technical Communications

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Editor: F. A. Sowan

Assistant Editors: E. G. Evans R. Barrie

Published by

Technical Information Department
Mullard Limited, Mullard House, Torrington Place, London, W.C.1
LANgham 6633

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Made and Printed in England by
WIGHTMAN AND COMPANY LIMITED, 1/3 BRIXTON ROAD, LONDON, S.W.9

Transistor Decoder Circuits for F.M. Stereo Broadcasting

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Mullard Research Laboratories

This article describes two transistor decoders for use with the F.C.C. approved (G.E.-Zenith) v.h.f. f.m. stereophonic broadcasting system.

One circuit employs two transistors, two semiconductor diodes, and is for use with valve circuits. The other retains the basic simplicity of the first circuit, but uses four transistors and operates by means of a switching process. It is suitable for valve or transistor circuits and provides inherent reverse compatibility.

A stereo indicator ('beacon') circuit is also described.

INTRODUCTION

Two simple valve-equipped decoders have already been described (Ref. 1). The present article describes the transistor counterparts of the valve-equipped decoders. A full discussion on transistor decoder circuits can be found in Ref. 2.

An attempt has been made to design:

(i) A simple transistor decoder for use with valve-equipped ratio detectors and audio amplifiers, and
(ii) A versatile decoder to operate from all normal ratio detectors, either valve or transistor, and to feed into any conventional amplifiers (valve or transistor).

The first decoder circuit (Fig. 1) is of particular use where it is difficult or impossible to obtain h.t. and l.t. supplies for a valve decoder. This difficulty is likely with a.c./d.c. equipment. The necessary power supply for a transistor decoder may readily be obtained from the cathode circuit of an output valve or by rectifying the heater voltage of the valve at the earthy end of the chain.

The second circuit (Fig. 3) will fulfil the same functions as the first decoder circuit but it has the added advantage that its output impedance is sufficiently low to drive a transistor audio amplifier. This circuit also provides inherent reverse compatibility.

To meet any demand for a visual indication that a stereo broadcast is in progress, a two-transistor circuit is described. This design is capable of switching on a 1·2W low-voltage lamp (Fig. 7).

SIMPLE TWO-TRANSISTOR DECODER

The circuit of the two-transistor decoder is shown in Fig. 1. It is designed primarily to operate from a valve ratio detector and is suitable only for valve-equipped audio amplifiers with high input impedances.

To achieve an overall gain of approximately unity, the complete multiplex signal is first amplified by an OC81

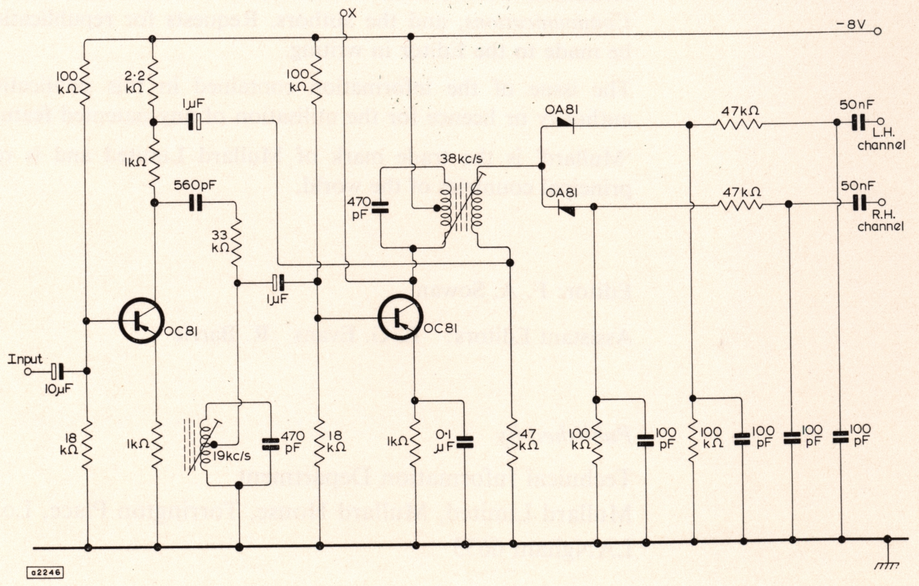
ox
−8V
100 kΩ
2·2 kΩ
100 kΩ
1μF
1kΩ
560pF
33 kΩ
1μF
38kc/s
470 pF
OA81
OA81
47kΩ
47kΩ
50nF
L.H. channel
50nF
R.H. channel
OC81
OC81
Input
10μF
18 kΩ
1kΩ
19kc/s
470 pF
18 kΩ
1kΩ
0·1 μF
47 kΩ
100 kΩ
100 pF
100 kΩ
100 pF
100 pF
100 pF
a2246

Fig. 1—Simple two-transistor decoder

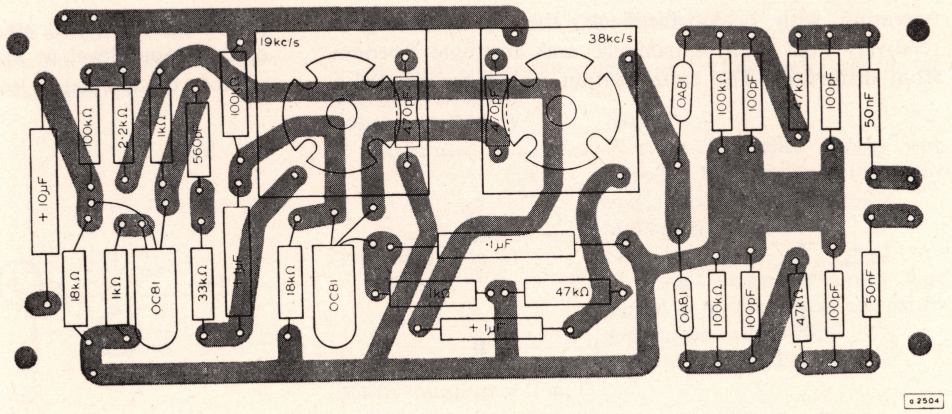
19kc/s
38kc/s
+10μF
100kΩ
2·2kΩ
1kΩ
560pF
100kΩ
470pF
470pF
OA81
100kΩ
100pF
47kΩ
100pF
50nF
·1μF
18kΩ
1kΩ
OC81
33kΩ
1μF
18kΩ
OC81
1kΩ
47kΩ
+1μF
OA81
100kΩ
100pF
47kΩ
100pF
50nF
a2504

Fig. 2—
Suggested printed board layout for simple decoder

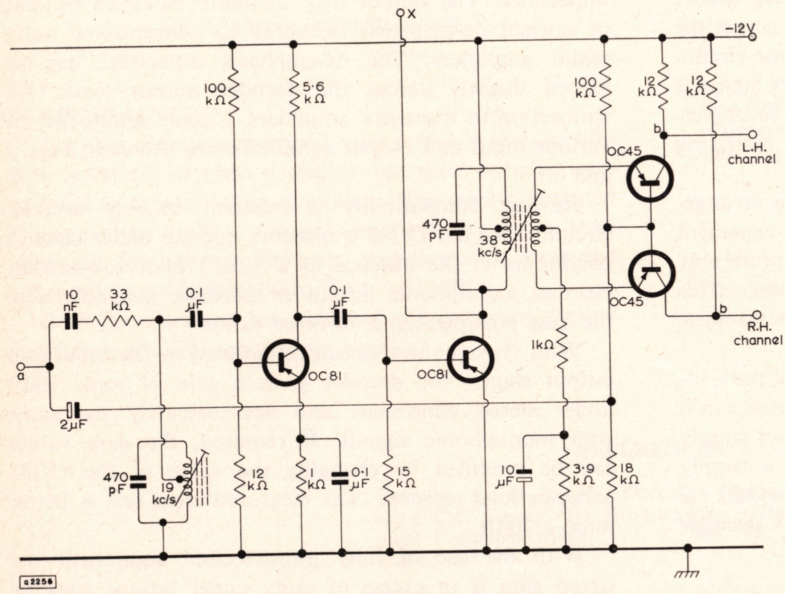
ox
−12V
100 kΩ
5·6 kΩ
100 kΩ
12 kΩ
12 kΩ
b
L.H. channel
OC45
470 pF
38 kc/s
OC45
10 nF
33 kΩ
0·1 μF
0·1 μF
1kΩ
b
R.H. channel
a
OC81
OC81
2μF
470 pF
19 kc/s
12 kΩ
1 kΩ
0·1 μF
15 kΩ
10 μF
3·9 kΩ
18 kΩ
a2256

Fig. 3—
Four-transistor decoder

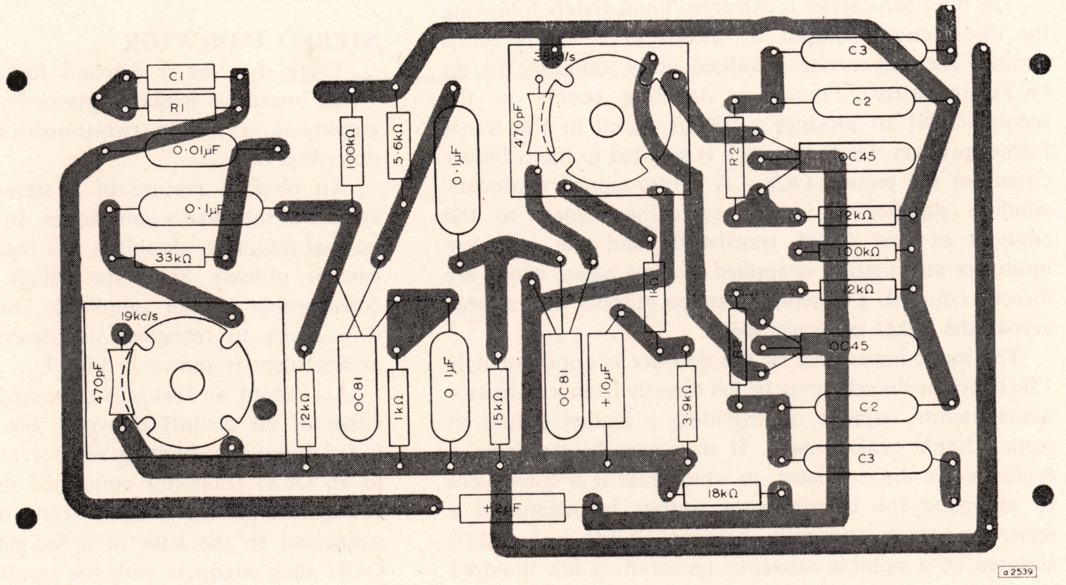
C1
R1
38kc/s
C3
C2
0·01μF
100kΩ
5·6kΩ
0·1μF
470pF
R2
OC45
0·1μF
12kΩ
100kΩ
33kΩ
12kΩ
19kc/s
470pF
12kΩ
OC81
1kΩ
0·1μF
15kΩ
OC81
+10μF
3·9kΩ
OC45
C2
C3
+2μF
18kΩ
a2539

Fig. 4—
Suggested printed board layout for four-transistor decoder

operating with heavy feedback, thereby providing a relatively high input impedance and adequate freedom from distortion. The entire output is fed by way of a phase correcting network to the 19kc/s circuit which extracts the pilot sub-carrier. Frequency doubling occurs in the second OC81, to produce a 38kc/s signal across the tuned primary of the transformer in the collector circuit. The requisite fraction of the amplified multiplex signal is connected to one end of the 38kc/s transformer secondary winding. Demodulation of the sidebands and matrixing occur in the diode circuits in the usual way.

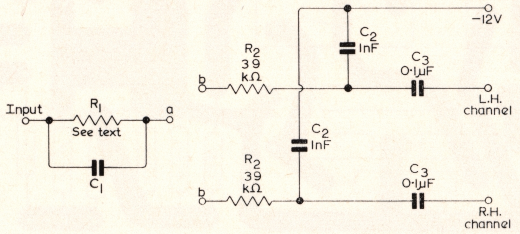

Fig. 5—Valve input and output circuits

Reverse compatibility is not inherent with this arrangement but can be readily achieved by the simple expedient of connecting the two outputs together, preferably immediately following the diodes themselves. This technique preserves the best possible signal-to-noise ratio for monophony.

The decoder will handle signals of up to 1·5V peak-to-peak at its input (corresponding to a discriminator e.m.f. of approximately 3V peak-to-peak) with a power supply of 8V at 2mA, or approximately 2·75V with a supply voltage of 12V at 3mA. The measured cross-talk is better than −20dB. A suggested layout for this decoder is shown in Fig. 2.

FOUR-TRANSISTOR DECODER

A more flexible and versatile decoder is illustrated in Fig. 3 operating with a 12V, 2·5mA supply.

The pilot sub-carrier is extracted immediately following the discriminator output by means of a 19kc/s tuned circuit. The sub-carrier is subsequently amplified by an OC81 transistor. Frequency doubling occurs in the second OC81 to produce a 38kc/s signal in the transformer primary winding, which is situated in the collector circuit of the second OC81. A centre-tapped secondary winding supplies anti-phase switching signals to the emitters of two OC45 transistors, and the complete multiplex information is applied to their bases, which are directly coupled. The separate stereo outputs thus appear across the 12kΩ collector loads.

The input impedance of the decoder is approximately 15kΩ and the decoder may be fed directly from a transistor discriminator, capable of providing a loaded output of some 750mV peak-to-peak. It may also be fed from a typical valve discriminator, in which case it is convenient to attenuate the discriminator output by means of a series resistance (typically between 3·3kΩ and 33kΩ) shunted by a suitable capacitor (generally a few hundred picofarads). Such an arrangement not only provides the correct input level at all multiplex frequencies but also reduces discriminator loading to an acceptable value.

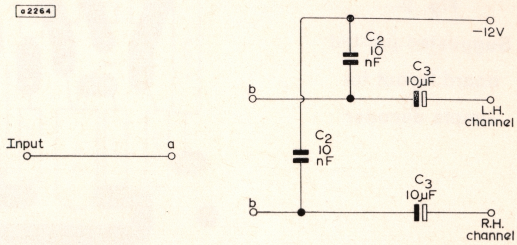

Fig. 6—Transistor input and output circuits

The output circuits are of approximately 12kΩ impedance. The output may therefore be taken by way of normal de-emphasis networks to conventional valve audio amplifiers. The de-emphasis capacitors can be placed directly across the decoder output loads, for connection to transistor amplifiers. Circuit details for the various input and output conditions are shown in Figs. 5 and 6.

Reverse compatibility is inherent in this decoder circuit, since the OC45 transistors operate under class A conditions in the absence of a 19kc/s pilot sub-carrier. Normal monophonic output is therefore available with the best possible signal-to-noise ratio.

With typical valve circuits connected to the input and output stages, the decoder gives a gain of some 10dB under stereo conditions and approximately the same with monophonic signals. If required, the gain values can be modified by changing the value of the OC45 collector load resistors. The measured cross-talk is better than −20dB.

With the use of fully transistorised equipment the stereo gain is in excess of unity under typical working conditions.

A suggested printed wiring board layout for this decoder is shown in Fig. 4.

STEREO INDICATOR

There may be a demand for an indication that a stereo broadcast is taking place. For this reason a circuit employing a simple two-transistor visual indicator is described (Fig. 7).

An obvious feature of a stereophonic broadcasting system is the 19kc/s sub-carrier. In a decoder employing normal frequency doubling, the regenerated 38kc/s signal can be utilised. Since the 38kc/s signal voltage is of considerably greater amplitude than the 19kc/s signal, it is easier to recognise its presence. A typical circuit arrangement is shown in Fig. 7.

An output at 38kc/s is extracted at a point 'X' from either of the circuits shown in Fig. 1 or 3. This output is fed through a limiting resistor and isolating capacitor to an OC81 transistor connected in the emitter-follower configuration. The output from the OC81 is directly connected to the base of a second OC81. The second OC81 thus conducts with the result that the small lamp in its collector circuit glows. In the absence of the 19kc/s sub-carrier and thus the 38kc/s output, the second transistor is cut off and the lamp is extinguished.

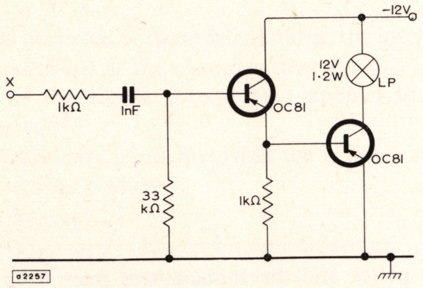

Fig. 7—Stereo indicator circuit

PERFORMANCE

The two decoders described were tested in conjunction with a variety of ratio detectors and their outputs were coupled to typical audio amplifiers. The results obtained indicate that the two circuits described are more than adequate for normal domestic purposes with measured cross-talk considerably better than −20dB.

Both decoders and the indicator circuit accept normal spreads in the transistor types used.

COIL DETAILS

Mullard Vinkor pot cores type LA2505 were used in the decoders described.

19kc/s coil (Fig. 1)	140mH
990 turns	43 s.w.g. enamelled copper wire tapped at 135 turns from the earthy end, tuned with 470pF±2%. Mullard type WF2948
19kc/s coil (Fig. 3)	140mH
990 turns	43 s.w.g. enamelled copper wire tapped at 40 turns from the earthy end, tuned with 470pF±2%. Mullard type WF2949
38kc/s transformer (Fig. 1)	
Secondary (wound first)	
120 turns	36 s.w.g. enamelled copper wire
Primary 35mH	
495 turns	43 s.w.g. enamelled copper wire, tapped at 60 turns from the start (collector end), tuned with 470pF±2% Mullard type WF2950
38kc/s transformer (Fig. 3)	
Primary 35mH	
495 turns	39 s.w.g. enamelled copper wire tapped at 60 turns from the start (collector end), tuned with 470pF±2% Mullard type WF2951
Secondary	
12 turns	39 s.w.g. enamelled copper wire centre tapped

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1. Browne, G. D. 'Simple Decoders (Adaptors) for use with the F.C.C. Stereo VHF Broadcasting System'. **Mullard Technical Communications,** Vol. 6, No. 59, August 1962, pp. 360 to 367.

2. Browne, G. D. 'Transistorised Decoders for FM Stereo'. **Hi-Fi News,** Vol. 8, No. 1, June 1963, pp. 38 to 44.

Capacitive Intermodulation in Dual-trace Oscilloscope Tubes

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In any c.r.t. with two or more electrostatic deflection systems, some degree of capacitive intermodulation between the systems may be encountered. This article shows the manner in which interaction is affected by (a) *the direct capacitances* (b) *variations in frequency and* (c) *the external circuit. A split beam tube has been examined for the purpose of the calculations but the reasoning is equally applicable to double-gun systems and to x-to-y intermodulation.*

INTRODUCTION

If a c.r.t. has two or more electrostatic deflection systems there may exist some form of intermodulation between the systems. This can occur in two basic forms, namely field intermodulation and capacitive intermodulation. Field intermodulation results directly from the effect of the electrostatic field, due to one set of deflector plates, upon the beam passing through the other system. The effect in any one system will be constant at all frequencies from d.c. upwards. Capacitive intermodulation is caused by signals induced at the deflector plates of one system, from the deflector plates of the other system, through capacitive coupling. It is the second of these causes, capacitive intermodulation, which is considered in this article. Although this article is based on the considerations for a split-beam tube the intermodulation effect will be present in double-gun tubes in a similar manner.

Other possible reasons for intermodulation are mutual inductance between leads within the tube, and couplings between leads, either capacitive or inductive, external to the tube. Inductive coupling within the tube and in well-constructed circuitry will almost invariably be negligible. Capacitive coupling external to the tube depends upon circuit layout and should be negligible, but otherwise can be dealt with directly as an increase in the cross-coupling capacitances.

In the early days of dual-trace oscillography the split beam tube was the only type of tube available: the double-gun was considered to present too many technical problems.

In the first split-beam tubes the y deflection system consisted of three plates as shown in Fig. 1a. The central plate was connected to a_3 and acted as a shield between the two beams. The outer plates, one on either side, acted as the deflector plates. Each beam was, then, asymmetrically deflected. With this arrangement the capacitive intermodulation between the beams could be ascertained from the capacitance between the two deflector plates and the capacitances from each deflector plate to earth. For the purpose of published data, the significant value was $c_{(y'-y'')}$ which can be seen from Fig. 1b.

In recent years, double-gun tubes have come into common use and, more recently, symmetrically deflected split beam tubes have been developed. The system of expressing intermodulation capacitance was unfortunately carried over from the old asymmetric tubes and published data often shows the capacitance $c_{(y1'+y2')-(y1''+y2'')}$. This capacitance has only limited practical significance and it is the purpose of this article to show the manner in which capacitive intermodulation is related to inter-electrode capacitances.

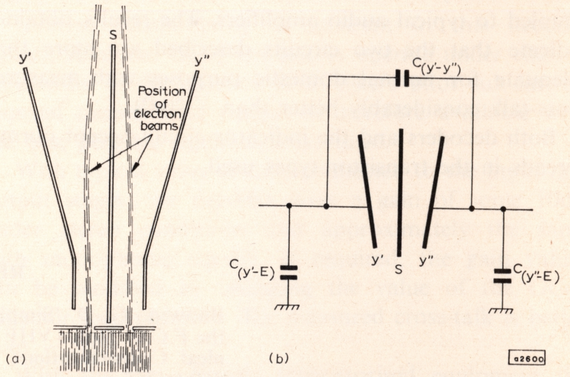

Fig. 1—Simplified structure of asymmetric split-beam deflection system, and the associated capacitances

While the calculations that follow are intended to apply to the dual trace tubes, they are equally applicable to capacitive intermodulation between x and y systems.

CAPACITANCE RELATIONSHIPS

In assessing capacitive intermodulation accurately there are seven admittances directly responsible for interaction which must be taken into account, namely:

(1) $Y_{(y1'-y1'')}$
(2) $Y_{(y1'-y2'')}$
(3) $Y_{(y2'-y1'')}$
(4) $Y_{(y2'-y2'')}$
(5) $Y_{(y1''-y2'')}$
(6) $Y_{(y1''-e)}$
(7) $Y_{(y2''-e)}$

The suffix numbers define the plate within each system, the primes define the system (or gun), and e indicates earth. Of these admittances, the first five are purely capacitive. The last two, however, include the output conductance of the scan output valves, and because of this it is simpler for the moment to consider each case as an admittance. The appropriate capacitances and admittances are shown in Fig. 2.

For the purposes of these calculations, the intermodulation voltage (V_{eff}) at the second system ($y_1''y_2''$) is derived in terms of the signal voltage (V_o) applied to the first system ($y_1'y_2'$).

The equivalent circuit involving the seven admittances is shown in Fig. 3 where

$$\left.\begin{aligned} A &= Y_{(y1'-y1'')} \\ B &= Y_{(y2'-y1'')} \\ C &= Y_{(y1'-y2'')} \\ D &= Y_{(y2'-y2'')} \end{aligned}\right\} \text{Direct intermodulating capacitances}$$

$$\left.\begin{aligned} E &= Y_{(y1''-e)} \\ F &= Y_{(y2''-e)} \end{aligned}\right\} \text{Plate-to-earth capacitances (including external capacitances)}$$

$$G = Y_{(y1''-y2'')}\} \text{ Plate-to-plate capacitance}$$

The instantaneous currents through these admittances are defined by the corresponding small letters, a, b, c, d, e, f, and g respectively.

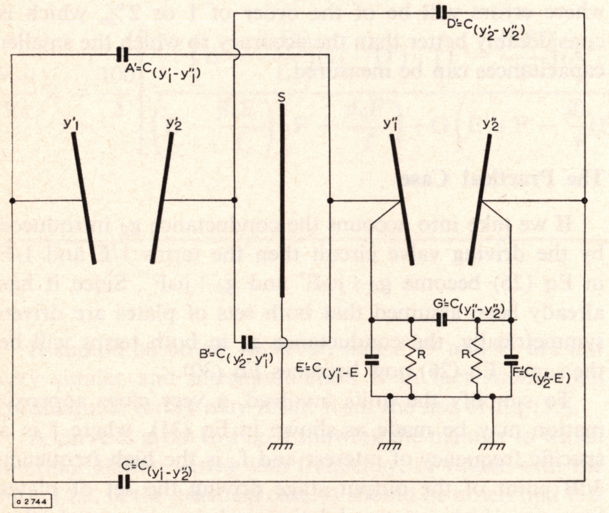

Fig. 2—Capacitances and conductances associated with the symmetrical deflection system. The resistor R represents the output resistance of the driving-stage, and is used in the calculation as the conductance g_d where $g_d = 1/R$

Applying Kirchoff's laws the following relationships are established:

$$a+g = e+b \qquad \ldots(1)$$
$$c+f = g+d \qquad \ldots(2)$$
$$Ff+Ee+Gg = 0 \qquad \ldots(3)$$
$$V_1 = Aa+Ee \qquad \ldots(4)$$
$$V_2 = Bb-Ee \qquad \ldots(5)$$
$$Aa = Cc+Gg \qquad \ldots(6)$$
$$V_2 = Ff+Dd. \qquad \ldots(7)$$

From Eq (4)

$$a = \frac{V_1-Ee}{A}. \qquad \ldots(8)$$

From Eq (5)

$$b = \frac{V_2+Ee}{B}. \qquad \ldots(9)$$

From Eqs (1), (8) and (9)

$$\frac{V_1-Ee}{A}+g = e+\frac{V_2+Ee}{B}. \qquad \ldots(10)$$

From Eq (7)

$$d = \frac{V_2-Ff}{D}. \qquad \ldots(11)$$

From Eqs (11) and (3)

$$d = \frac{V_2+Ee+Gg}{D}. \qquad \ldots(12)$$

From Eq (6)

$$c = \frac{Aa-Gg}{C}. \qquad \ldots(13)$$

From Eqs (13) and (4)

$$c = \frac{V_1-Ee-Gg}{C}. \qquad \ldots(14)$$

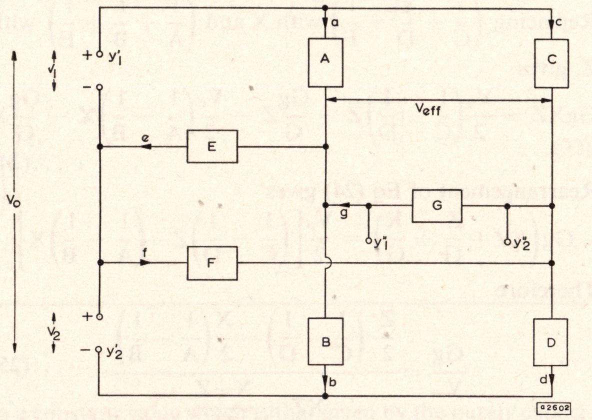

Fig. 3—Equivalent circuit of plate system; the admittances are defined in the text

From Eqs (2), (12) and (14)

$$\frac{V_2-Ff}{D}+g = f+\frac{V_1-Ee-Gg}{C}. \qquad \ldots(15)$$

From Eq (3)

$$Ff = -(Ee+Gg) \qquad \ldots(16)$$

and

$$f = \frac{-(Ee+Gg)}{F}. \qquad \ldots(17)$$

From Eqs (15), (16) and (17)

$$\frac{V_2+Ee+Gg}{D}+g = \frac{V_1-Ee-Gg}{C}-\frac{Ee+Gg}{F} \qquad \ldots(18)$$

which may be rearranged in the form:

$$Ee+Gg = \frac{\dfrac{V_1}{C}-\dfrac{V_2}{D}-g}{\left(\dfrac{1}{D}+\dfrac{1}{C}+\dfrac{1}{F}\right)}. \qquad \ldots(19)$$

Eq (10) may be re-written to give:

$$\frac{V_1-Ee}{A}+g = \frac{Ee}{E}+\frac{V_2+Ee}{B}. \qquad \ldots(20)$$

This may now be rearranged to give:

$$\mathrm{Ee} = \frac{\frac{V_1}{A} - \frac{V_2}{B} + g}{\left(\frac{1}{A} + \frac{1}{B} + \frac{1}{E}\right)}. \qquad \ldots(21)$$

Subtracting Eq (21) from Eq (19)

$$\mathrm{Gg} = \frac{\frac{V_1}{C} - \frac{V_2}{D} - g}{\left(\frac{1}{C} + \frac{1}{D} + \frac{1}{F}\right)} - \frac{\frac{V_1}{A} - \frac{V_2}{B} + g}{\left(\frac{1}{A} + \frac{1}{B} + \frac{1}{E}\right)}. \qquad \ldots(22)$$

This expression is somewhat simplified if we consider the case of balanced symmetrical input to the $y_{1'}y_{2'}$ plates. Referring to Fig. 3 we can now consider that $V_1 = V_2 = V_o/2$ where V_o is the voltage applied between $y_{1'}$ and $y_{2'}$. Hence,

$$\mathrm{Gg} = \frac{\frac{V_o}{2}\left(\frac{1}{C} - \frac{1}{D}\right) - g}{\left(\frac{1}{C} + \frac{1}{D} + \frac{1}{F}\right)} - \frac{\frac{V_o}{2}\left(\frac{1}{A} - \frac{1}{B}\right) + g}{\left(\frac{1}{A} + \frac{1}{B} + \frac{1}{E}\right)}. \qquad \ldots(23)$$

Replacing $\left(\frac{1}{C} + \frac{1}{D} + \frac{1}{F}\right)$ with X and $\left(\frac{1}{A} + \frac{1}{B} + \frac{1}{E}\right)$ with Z, gives

$$\mathrm{GgXZ} = \frac{V_o}{2}\left(\frac{1}{C} - \frac{1}{D}\right)Z - \frac{\mathrm{Gg}}{G}Z - \frac{V_o}{2}\left(\frac{1}{A} - \frac{1}{B}\right)X - \frac{\mathrm{Gg}}{G}X \qquad \ldots(24)$$

Rearrangement of Eq (24) gives

$$\mathrm{Gg}\left(XZ + \frac{Z}{G} + \frac{X}{G}\right) = \frac{V_o}{2}\left[\left(\frac{1}{C} - \frac{1}{D}\right)Z - \left(\frac{1}{A} - \frac{1}{B}\right)X\right].$$

Therefore

$$\frac{\mathrm{Gg}}{V_o} = \frac{\frac{Z}{2}\left(\frac{1}{C} - \frac{1}{D}\right) - \frac{X}{2}\left(\frac{1}{A} - \frac{1}{B}\right)}{XZ + \frac{X+Z}{G}}. \qquad \ldots(25)$$

But Gg will be the voltage appearing between the $y_{1''}$ and $y_{2''}$ plates. This is the effective intermodulation voltage and will be denoted as V_{eff}.

Substituting once again for the terms X and Z, the percentage intermodulation between the two deflection systems will be given by Eq (26) on page 209.

The Simplified Case

It is often convenient, and certainly much simpler, to consider the condition where the second set of deflector plates is open-circuited. The conductance due to the driving stages is ignored and all of the admittances become purely capacitive. This represents the worst case of intermodulation obtainable for any given set of capacitances and is a limit figure for the c.r.t.

Each admittance may be replaced by the appropriate value of ωC and since ω appears in the same order in both numerator and denominator the percentage intermodulation, as shown in Eq (26), can be written as in Eq (27) on page 209, where the prime associated with each symbol indicates that it represents the actual value of capacitance (for example $A = 1/j\omega A'$).

The expression may be further simplified if we choose to ignore the term G′ which represents the capacitance between the plates of the second system. This in itself could result in an error of the order of 30% in the typical case of the Mullard E10-11GH if tube capacitances only were being considered. However, it must be remembered that in practice the deflection circuit output capacitances will appear in parallel with E′ and F′, tending to reduce the error to something much closer to 10%.

Eq (27) will now become

$$\frac{V_{eff}}{V_o}\% = \tfrac{1}{2}\left[\frac{(C'-D')}{(C'+D'+F')} - \frac{(A'-B')}{(A'+B'+E')}\right] \times 100\%. \qquad \ldots(28)$$

From this it can be seen that it is not so much the actual values of A′, B′, C′, and D′ which are significant, but rather the relationship between them.

A much more reasonable approximation may be derived from the fact that the capacitances A′, B′, C′, and D′ are almost invariably small compared with E′ and F′ and Eq (27) may be reduced to

$$\frac{V_{eff}}{V_o}\% = \tfrac{1}{2}\left[\frac{E'(C'-D')-F'(A'-B')}{E'F'+G'(E'+F')}\right] \times 100\% \qquad \ldots(29)$$

where errors will be of the order of 1 or 2%, which is considerably better than the accuracy to which the smaller capacitances can be measured.

The Practical Case

If we take into account the conductance g_d introduced by the driving valve circuit then the terms 1/E and 1/F in Eq (26) become $g_d+j\omega E'$ and $g_d+j\omega F'$. Since it has already been assumed that both sets of plates are driven symmetrically, the conductance g_d in both terms will be the same. Eq (26) now becomes Eq (30).

To simplify the units involved, a very close approximation may be made as shown in Eq (31), where f is a specific frequency of interest and f_o is the high frequency 3dB point of the output stage driving the set of plates between which intermodulation is being measured (that is, $f_o = g_d/2\pi E'$). The assumption is made in Eq (31) that the capacitances E′ and F′ are similar in value, and since these values will include strays and valve output capacitances in a balanced arrangement, this is a reasonable assumption.

Once again, if A′, B′, C′, and D′ are small compared with E′ and F′, a much more practical expression may be derived as in Eq (32).

It is interesting to note that if E′ and F′ are in fact identical then a further simplification may be made:

$$\frac{V_{eff}}{V_o}\% = \frac{100}{2}\left[\frac{(C'-D')-(A'-B')}{\left(E' - \frac{jf_oE'}{f}\right)+2G'}\right]\%. \qquad \ldots(33)$$

Since the values of the capacitances E′ and F′ determine the bandwidth of the output stage of the amplifier it may be reasonable in some cases to ensure by means of padding-capacitances that these are equal. Thus both sides of the output stage would have the same bandwidth, and the possibility of high frequency distortions would be reduced.

$$\frac{V_{eff}}{V_o}\% = \tfrac{1}{2}\left[\frac{\left(\frac{1}{A}+\frac{1}{B}+\frac{1}{E}\right)\left(\frac{1}{C}-\frac{1}{D}\right) - \left(\frac{1}{C}+\frac{1}{D}+\frac{1}{F}\right)\left(\frac{1}{A}-\frac{1}{B}\right)}{\left(\frac{1}{A}+\frac{1}{B}+\frac{1}{E}\right)\left(\frac{1}{C}+\frac{1}{D}+\frac{1}{F}\right)+\frac{1}{G}\left(\frac{1}{A}+\frac{1}{B}+\frac{1}{C}+\frac{1}{D}+\frac{1}{E}+\frac{1}{F}\right)}\right] \times 100\%. \qquad \ldots(26)$$

$$\frac{V_{eff}}{V_o}\% = \tfrac{1}{2}\left[\frac{(A'+B'+E')(C'-D')-(C'+D'+F')(A'-B')}{(A'+B'+E')(C'+D'+F')+G'(A'+B'+C'+D'+E'+F')}\right] \times 100\%. \qquad \ldots(27)$$

$$\frac{V_{eff}}{V_o}\% = \frac{100}{2}\left[\frac{\left(A'+B'+E'-\frac{jg_d}{\omega}\right)(C'-D')-\left(C'+D'+F'-\frac{jg_d}{\omega}\right)(A'-B')}{\left(A'+B'+E'-\frac{jg_d}{\omega}\right)\left(C'+D'+F'-\frac{jg_d}{\omega}\right)+G'\left(A'+B'+C'+D'+E'+F'-\frac{2jg_d}{\omega}\right)}\right]\%. \qquad \ldots(30)$$

$$\frac{V_{eff}}{V_o}\% = \frac{100}{2}\left[\frac{\left(A'+B'+E'-\frac{jf_oE'}{f}\right)(C'-D')-\left(C'+D'+F'-\frac{jf_oF'}{f}\right)(A'-B')}{\left(A'+B'+E'-\frac{jf_oE'}{f}\right)\left(C'+D'+F'-\frac{jf_oF'}{f}\right)+G'\left(A'+B'+C'+D'+E'+F'-\frac{jf_o}{f}(E'+F')\right)}\right]\%. \qquad \ldots(31)$$

$$\frac{V_{eff}}{V_o}\% = \frac{100}{2}\left[\frac{\left(E'-\frac{jf_oE'}{f}\right)(C'-D')-\left(F'-\frac{jf_oF'}{f}\right)(A'-B')}{\left(E'-\frac{jf_oE'}{f}\right)\left(F'-\frac{jf_oF'}{f}\right)+G\left(E'+F'-\frac{jf_o}{f}(E'+F')\right)}\right]\%. \qquad \ldots(32)$$

It should be noted, however, that if E′ and F′ are not very similar and intermodulation is in fact small, then considerable errors may result from the use of Eq (33).

A curve is given in Fig. 4 showing the manner in which intermodulation varies with frequency, or rather with the ratio f/f_o, in the practical case. It should be noted that it is the reciprocal of this ratio which appears in the calculations. It can be seen that at low frequencies the intermodulation tends to zero since the capacitances E′ and F′ become effectively short-circuited by the output conductance of the driving source. At high frequencies the curve flattens to a constant value which is that given by the purely capacitive case considered earlier.

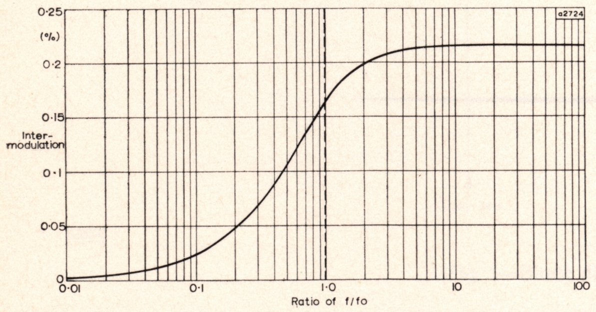

Fig. 4—Intermodulation as a function of frequency

If it is considered that both driven plates and the plates receiving cross-modulation are supplied by circuits having the same bandwidth then the vertical dotted line in Fig. 4 indicates the 3dB point where $f = f_o$. For most practical purposes, this is the highest frequency of interest in any given system.

Reverse Intermodulation

It is of interest at this point to consider the expression for the intermodulation voltage between the $y_{1'}y_{2'}$ plates caused by a signal applied to the $y_{1''}y_{2''}$ plates. In the approximate form corresponding to Eq (33) this will be

$$\frac{V_{eff}}{V_o'}\% = \frac{100}{2}\left[\frac{(A'-C')-(B'-D')}{H'-\left(\frac{jf_oH'}{f}\right)+2K}\right]\% \qquad \ldots(34)$$

where H′ and K′ are the capacitances $c_{(y1'-e)}$ or $c_{(y2'-e)}$, and $c_{(y1'-y2')}$ respectively. From Eqs (33) and (34) it may be stated that, if $(A'+D') = (B'+C')$ then intermodulation in both directions will be zero; that is, there will be no modulation in either trace. This relies on the assumption which led to the simplification of the expression, namely that $E' = F'$. If E′ is not equal to F′ then intermodulation will be zero in both directions only when $A' = B' = C' = D'$.

Example

A typical practical case has been worked and is illustrated by curve A in Fig. 5. The capacitance values used were:

A′	0·03pF	E′	3·0pF
B′	0·05pF	F′	3·0pF
C′	0·01pF	G′	0·6pF
D′	0·02pF		

The curve A illustrates the behaviour of the intermodulation as the external capacitance between each plate and earth is increased from zero to 12pF. This curve shows the general behaviour rather than absolute values of intermodulation. It has therefore been calculated in the simple form from Eq (33), for the 3dB point, that is, where $f = f_0$.

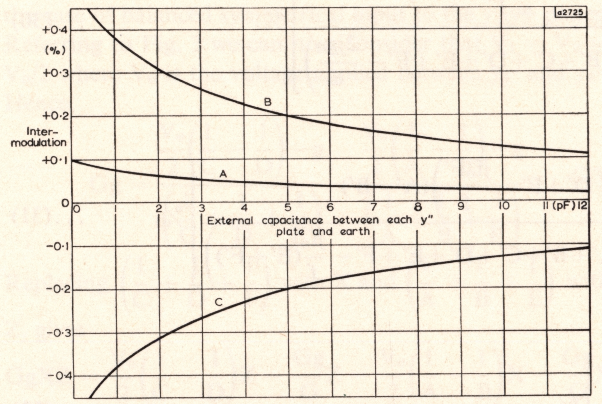

Fig. 5—The effect of external y-plate capacitance on intermodulation

Since the capacitances A′, B′, C′, and D′ are the significant values in the calculation of intermodulation, the limit values of these capacitances must be considered. If the assumption is made that each of these capacitances may vary between zero and 0·05pF, then the worst cases of intermodulation will occur when B′ and C′ are zero and A′ and D′ are at a maximum, or vice versa. These two limit cases are shown by curves B and C. The use of the negative sign in association with the percentage intermodulation indicates phase reversal of the modulation signal relative to the signal causing the intermodulation.

TUBE SPECIFICATION

It has been shown that to define intermodulation with any degree of accuracy it would be necessary to know the actual value of four capacitances for each individual tube, in addition to those normally published. Since each of these capacitances would be subject to normal manufacturing tolerances, which, it has been shown, cause considerable variation in intermodulation, it is not possible to publish a practical general value. If, on the other hand, maximum and minimum values were quoted for each of these four additional capacitances it would still only be possible to define the worst case of intermodulation possible. If we consider the case which would give the worst intermodulation from Eq (33) then (B′+C′) will be at a maximum, while (A′+D′) are at a minimum, or vice versa. If we now say that the minimum value for any of the capacitances is zero it would make no difference if we wrote the numerator as A′+B′+C′+D′ since either A′ and D′, or B′ and C′, are now zero. The generally published value $c_{(y1'+y2')-(y1''+y2'')}$ is in fact identical to A′+B′+C′+D′.

Therefore it can be said that if the published value of $c_{(y1'+y2')-(y1''+y2'')}$ is suitably low, then intermodulation will be satisfactory. A high value of published capacitance does not, however, signify a large degree of intermodulation.

Therefore, in recent published data the maximum magnitude of intermodulation signal appearing at the screen for a given applied signal amplitude is quoted for the condition where the modulated plates are effectively open-circuited. For most users this is the most convenient way of presenting information on intermodulation. For special applications it can be seen from the article that zero intermodulation may be obtained by suitably trimming the appropriate capacitances.

Timebases for Sampling Oscilloscopes

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Mullard Semiconductor Measurement and Application Laboratory

Trigger, timebase and scanning circuits for a sampling oscilloscope are described in this article. The effective time scale achieved is down to 0·5*ns/cm.*

INTRODUCTION

This article describes the trigger, timebase and scanning circuits of a practical sampling oscilloscope, developed as a general purpose instrument giving effective time scales down to 0·5ns/cm. The circuits described constitute an inexpensive attachment for use with any existing oscilloscope, but they are also suitable for incorporation into a complete instrument. A later article will describe the signal circuits for sampling.

A full description of sampling systems has been given in a previous article (Ref. 1) but a block diagram of the timing section is given in Fig. 1. The circuits are fired by a trigger pulse which is time-locked to the signal and precedes the part of the signal waveform to be examined. They produce a series of pulses, sometimes called a 'slewed' pulse, whose delay relative to the input trigger progressively increases for each successive trigger. This progression is under the control of a 'staircase generator', which also provides the horizontal deflection voltage for the c.r.t. Each time the staircase generator resets, the delay returns to the minimum value, and the cycle is repeated. These pulses subsequently fire the sampling-pulse (or "strobe-pulse") generator to sample the signal.

The delay variation through each complete cycle of the staircase corresponds to the effective timebase length on the c.r.t. display. The start of the timebase can be delayed by a variable 'trigger' delay to permit the required portion of the displayed waveform to be selected. This delay has a maximum value of about 1μs and a minimum value of about 100ns. In simplified form, the major timing waveforms are shown in Fig. 2. The system described meets the following specifications:

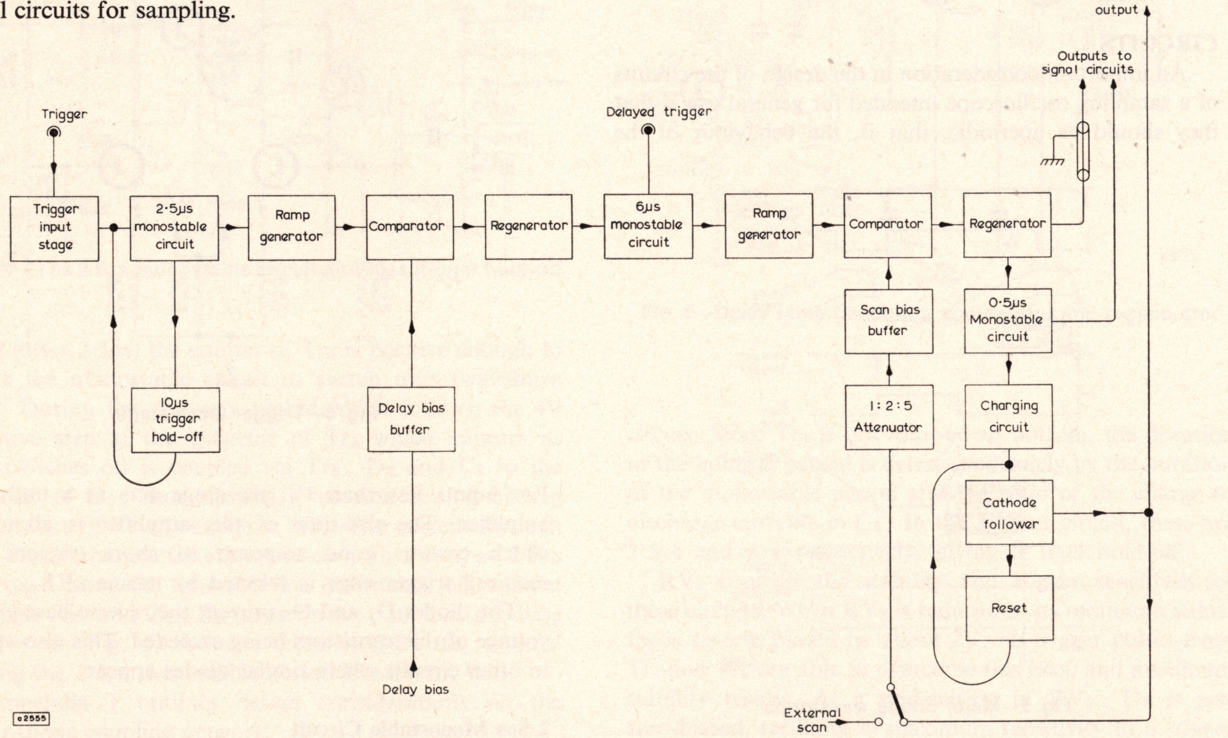

Fig. 1—Block diagram of timing circuits

Trigger Requirements

Amplitude: 50mV to 20V for all triggers $>$ 10ns duration or $>$ 0·50Vns area for triggers $<$ 10ns duration.

Rate:	10c/s to 20Mc/s (hold-off circuit operates above 100kc/s). Randomly spaced trigger pulses can be accepted.
Polarity:	Positive or negative.
Input capacitance:	Approx. 20pF.
Input resistance:	Approx. 5kΩ.

Trigger Delay

Ranges:	100ns or 1μs variation, continuously variable by means of 10-turn Helipot.
Calibration error:	< ±2% of range.
Minimum delay:	< 120ns from normal trigger input socket; < 50ns from 'Delayed Trigger' socket.
Intrinsic jitter:	< 1:10 000, or < 50ps, whichever is greater.
Delayed trigger output:	3V positive pulse.

Timebase

Sweep speeds:	Ten calibrated sweep speeds from 0·5μs/cm to 0·5ns/cm in 1:2:5 sequence.
Linearity error:	< ±2%.
Samples per sweep:	Approx. 150 to 1500.

The various parts of this circuit shown in block diagram form in Fig. 1 are described more fully below.

CIRCUITS

An important consideration in the design of the circuits of a sampling oscilloscope intended for general use is that they should be aperiodic, that is, the behaviour of the system following a trigger pulse should be entirely independent of the period between successive triggers, within the design limits. For this reason, the circuits are d.c. coupled, or, in some cases, coupled via time-constants which are small compared to the minimum time between the triggers in that part of the circuit. The design has been greatly facilitated in this respect by the provision of several supply rails.

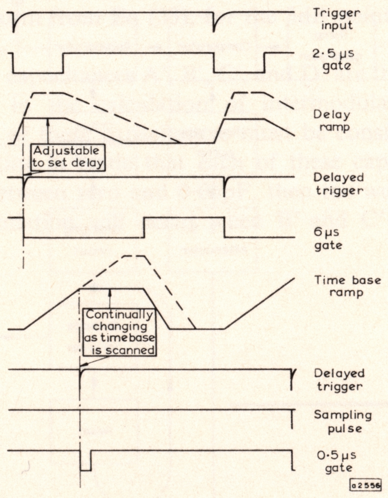
Trigger input
2·5 μs gate
Delay ramp
Adjustable to set delay
Delayed trigger
6 μs gate
Time base ramp
Continually changing as timebase is scanned
Delayed trigger
Sampling pulse
0·5 μs gate
a2556

Fig. 2—Major timing waveforms

The circuits are flexible enough to permit the system performance to be changed easily should the need arise. This results in some sections of the present design being more complicated than is necessary. Some simplifications are, however, suggested later in the article. The circuits shown in Figs. 3 to 13 are fully toleranced and have been reproduced several times. Many of the circuits described have applications other than the original one, and some of these are suggested.

Trigger Input Stage

Fig. 3 shows the circuit of the trigger input stage which comprises the long-tailed pair Tr_1-Tr_2. The input is d.c. coupled to Tr_1 via R_1 and R_3 ; this network is capacitance-compensated by C_1. The circuit behaves as a slicer to signals greater than 1V(pk) in amplitude, the slicing level being set by RV_1. The collector voltage swing is limited to about 1V by the tail current of 5mA flowing in 220Ω.

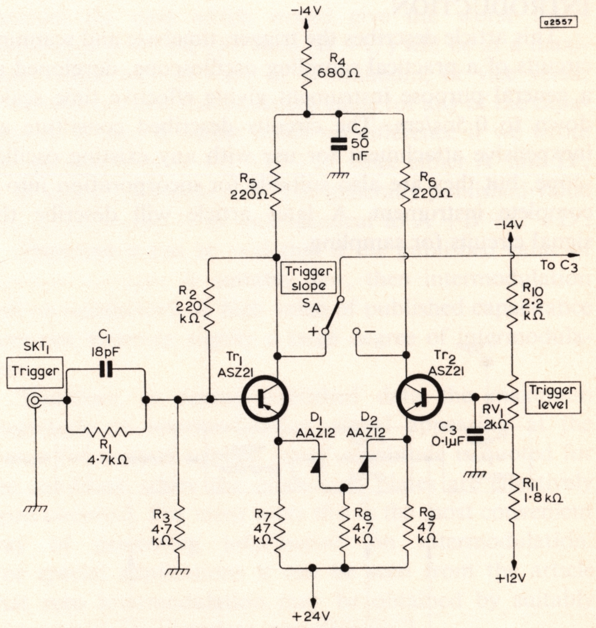
a2557
−14V
R4 680Ω
C2 50 nF
R5 220Ω
R6 220Ω
−14V
To C3
R2 220 kΩ
Trigger slope
SA
+
−
R10 2·2 kΩ
SKT1
Trigger
C1 18pF
R1 4·7kΩ
Tr1 ASZ21
Tr2 ASZ21
Trigger level
RV1 2kΩ
C3 0·1μF
D1 AAZ12
D2 AAZ12
R11 1·8 kΩ
R3 4·7 kΩ
R7 47 kΩ
R8 4·7 kΩ
R9 47 kΩ
+12V
+24V

Fig. 3—Trigger input stage

For inputs less than 1V, the stage acts as a unity-gain amplifier. The rise-time of this amplifier is about 4ns which ensures good response to short triggers. The required trigger edge is selected by means of S_A.

The diodes D_1 and D_2 prevent the reverse base-emitter voltage of the transistors being exceeded. This also applies to other circuits where similar diodes appear.

2·5μs Monostable Circuit

The lower half of Fig. 4 shows the 2·5μs monostable circuit which comprises Tr_5 , Tr_6 and the constant-current transistor Tr_{54}. Fig. 4 is an emitter-timed monostable circuit, described in detail in Ref. 2, having the 'linear-recovery' system described under the heading 'Modifications' in this reference.

In the quiescent state, Tr_6 and Tr_{54} are conducting. The collector of Tr_6 is caught at about −1·9V by means of D_8 and Z_2+Z_3. A trigger pulse from the input stage, applied via C_3 and D_3 , causes the monostable to switch into its quasi-stable state, when the collector current (approx. 10mA) of Tr_{54} is routed into Tr_5 via C_7 and D_4. The diode D_5 remains cut-off.

There is thus produced a positive step of approximately 4V at the collector of Tr_5 and hence at the base of Tr_6. This is shown in waveform W1. (Appendix 3 on page 224 gives notes on the waveforms.) C_7 then charges until (after 2·5μs) the emitter of Tr_6 is positive enough to cause the monostable circuit to switch over (waveform W2). During the recovery period which follows, the 4V negative step at the collector of Tr_5 which appears as Tr_5 switches off is coupled via Tr_6 , D_6 and C_7 to the cathode of D_5 , thus turning it on and reverse-biasing the emitter of Tr_{54} (waveform W3). The current through R_{22} thus recharges C_7 almost linearly in a further 2·5μs approx. During the time that Tr_6 is switched off, current through R_{21} and Z_2+Z_3 turns on D_7 , so that the base of Tr_7 (in Fig. 5) switches from +13·2V to +10·8V during the 2·5μs monostable period (waveform W4).

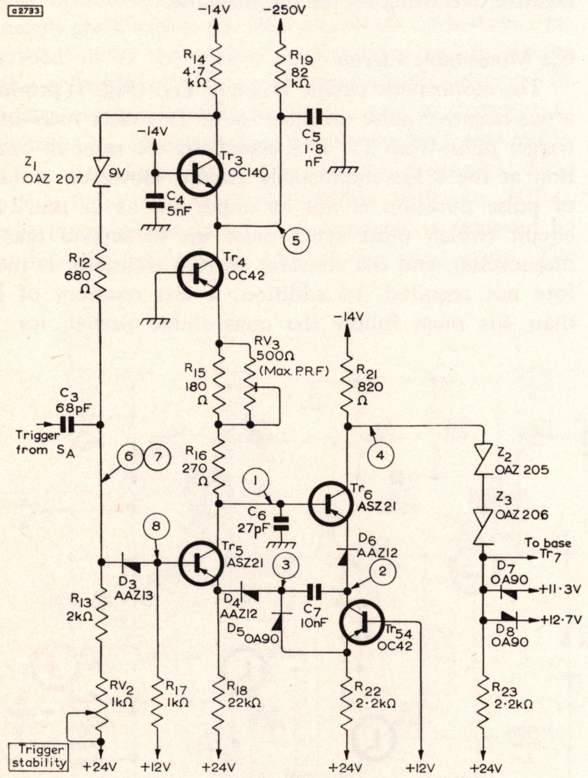
a2733
−14V
−250V
R14 4·7 kΩ
R19 82 kΩ
−14V
C5 1·8 nF
Z1 OAZ 207
9V
Tr3 OC140
C4 5nF
5
R12 680 Ω
Tr4 OC42
−14V
RV3 500Ω (Max. P.R.F)
R15 180 Ω
R21 820 Ω
C3 68pF
Trigger from SA
6
7
R16 270 Ω
4
Z2 OAZ 205
1
Tr6 ASZ21
Z3 OAZ 206
C6 27pF
8
To base Tr7
Tr5 ASZ21
3
D6 AAZ12
2
D7 OA90
+11·3V
D3 AAZ13
D4 AAZ12
C7 10nF
R13 2kΩ
D5 OA90
Tr54 OC42
+12·7V
D8 OA90
RV2 1kΩ
R17 1kΩ
R18 22kΩ
R22 2·2kΩ
R23 2·2kΩ
Trigger stability
+24V
+12V
+24V
+24V
+12V
+24V

Fig. 4—The 2·5μs monostable circuit and 10μs trigger hold-off

Appendix 1 outlines design considerations on the zener-diode coupling network.

10μs Trigger Hold-off Circuit

A maximum sampling rate of 100kc/s was fixed because of certain considerations in the signal circuits. If the trigger rate exceeds this, the timing circuits must 'count-down'. To ensure reliable triggering under these conditions, a trigger hold-off system comprising Tr_3 and Tr_4 is used, as shown in the upper half of Fig. 4.

With the monostable circuit Tr_5 , Tr_6 , Tr_{54} in its quiescent state, the collector current of Tr_5 is about 0·5mA which is a keepalive current through R_{18}. This current also flows out of the collector of Tr_4; the current in R_{19} , however, is greater than 0·5mA, so that the emitter of Tr_3 is forward biased, and caught at −14V. When the monostable circuit fires, the collector current of Tr_4 rises to about 10mA, which exceeds the current available in R_{19} , so that C_5 charges (waveform W5) and Tr_3 is switched off. The positive step which thus appears at the collector of Tr_3 is coupled to the cathode of D_3 , blocking the transmission of further triggers to the monostable (waveforms W6, 7 and 8; waveforms W7 and W8 show the blocking action at 1Mc/s).

When the monostable conduction period ends, C_5 discharges via R_{19} until Tr_3 once again conducts, and allows a further trigger pulse to pass to the monostable circuit. Since Tr_4 is not allowed to bottom, the duration of the hold-off period is determined solely by the duration of the monostable period and the ratio of the charge to discharge currents in C_5. In the present circuit, these are 2·5μs and 3:1 respectively, giving a 10μs hold-off.

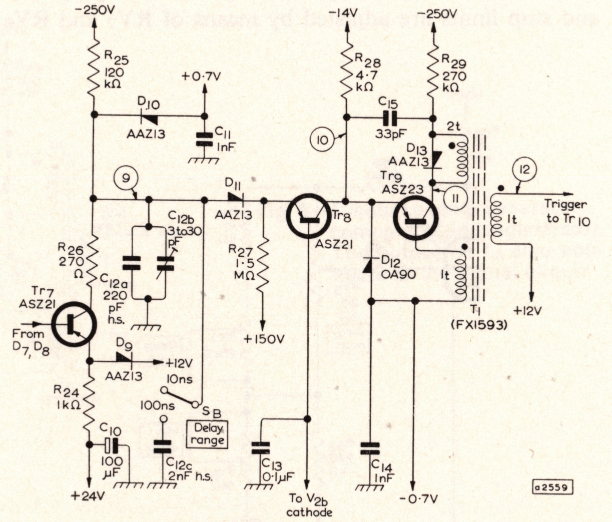
−250V
R25 120 kΩ
+0·7V
D10 AAZ13
C11 1nF
−14V
R28 4·7 kΩ
−250V
R29 270 kΩ
C15 33pF
10
2t
D13 AAZ13
Tr9 ASZ23
11
12
9
D11 AAZ13
C12b 3to30 pF
Tr8 ASZ21
Trigger to Tr10
1t
R26 270 Ω
C12a 220 pF h.s.
R27 1·5 MΩ
D12 OA90
1t
Tr7 ASZ21
From D7, D8
T1 (FX1593)
+12V
+150V
D9 AAZ13
+12V
10ns
100ns
SB
Delay range
R24 1kΩ
C10 100 μF
C12c 2nF h.s.
C13 0·1μF
C14 1nF
+24V
To V2b cathode
−0·7V
a2559

Fig. 5—Delay ramp generator, comparator and regenerator

RV_2 controls the stability and trigger sensitivity of these circuits. When RV_2 is reduced to its minimum value, D_3 is reverse biased by about 2V; no trigger pulses from Tr_1 and Tr_2 are able to overcome this bias, and maximum stability results. At a mid-setting of RV_2 , D_3 is just zero-biased, resulting in maximum sensitivity to a trigger pulse. Further rotation causes the system to free-run, at a nominal frequency of 100kc/s adjustable by RV_3 , which determines the monostable period.

Delay Ramp Generator and Comparator

The circuit of the delay ramp generator and comparator is shown in the first part of Fig. 5. In the quiescent state, Tr_7 is cut-off. The current through R_{24} flows into D_9 , and the current through R_{25} from D_{10}. The anode of D_{11}

is thus at approximately +0·2V. A bias applied to the base of Tr_8, the comparator, holds the emitter at a potential which can be varied between approximately +0·2V and +5·2V. D_{11} is thus reverse-biased.

The negative pulse from the monostable circuit on the base of Tr_7 switches Tr_7 on, and the collector current rapidly rises to approximately 12mA, defined by R_{24}. Since this exceeds the current in R_{25}, C_{12} begins to charge and D_{10} becomes reverse-biased. Above a potential of 10·5V the charging of C_{12} is very nearly linear. Tr_8 turns on after a time determined by the value of the charging current, the value of C_{12} and the bias voltage on the base of Tr_8.

At the end of the monostable conduction period, C_{12} discharges via R_{25} until D_{10} 'catches'. Two ranges are provided, giving a delay variation of 100ns or 1μs for a bias variation of approximately 5V. The delay is set by means of the delay multiplier Helipot RV_9 (Fig. 6). Start and stop limits are adjusted by means of RV_7 and RV_8.

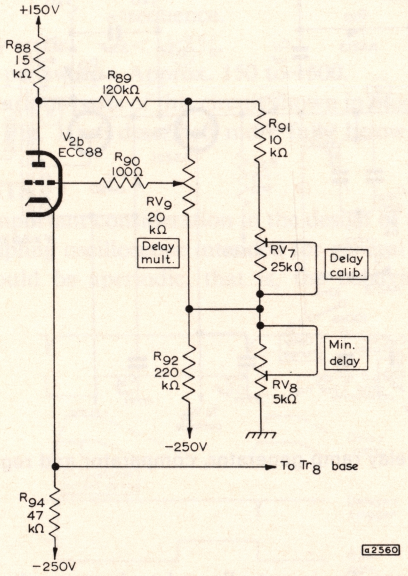
+150V
R88 15 kΩ
R89 120kΩ
V2b ECC88
R90 100Ω
R91 10 kΩ
RV9 20 kΩ
Delay mult.
RV7 25kΩ
Delay calib.
Min. delay
R92 220 kΩ
RV8 5kΩ
-250V
To Tr8 base
R94 47 kΩ
-250V
a2560

Fig. 6—Delay multiplier and buffer amplifier

The cathode-follower V_{2b} is used to minimise loading on RV_9 and thus ensure good linearity of the multiplier scale. The linearity of the ramp generated by the circuit of Fig. 5 is discussed in Appendix 2 on page 222. Waveform W9 shows the voltage across C_{12} on the 1μs delay range and waveform W9a corresponds to the 100ns range.

Regenerator Circuit

The avalanche transistor, Tr_9 in Fig. 5, is used to produce a standard trigger pulse to fire the following stage, from the positive step which appears at the collector of Tr_8. In the quiescent state, the current in R_{28} holds D_{12} in conduction; the emitter of Tr_9 is thus reverse-biased. Its collector remains at the avalanche potential of about −25V. When Tr_8 switches on, the emitter of Tr_9 is forward-biased (waveform W10) causing avalanche regeneration around the loop formed by Tr_9, Tr_1 and C_{15}. This produces a narrow negative spike at the output winding (waveform W12). A feedback winding in the base improves the stability of the output pulse against variations in the speed of the edge from Tr_8 as the TIME/CM control is varied.

Tr_9 remains bottomed until the end of the monostable period, when C_{15} recharges via R_{29} until the avalanche potential is reached (waveform W11), and D_{13} prevents positive overswing on the output pulse.

6μs Monostable Circuit

The monostable circuit Tr_{10} and Tr_{11} (Fig. 7) produces a 6μs negative pulse on the base of Tr_{12} after receiving a trigger pulse from T_1. It is essentially the same in operation at the 2·5μs monostable circuit. However, stability of pulse duration is not as important as in the 2·5μs circuit (which must synchronise up to several tens of megacycles), and the constant current transistor is therefore not required. In addition, a fast recovery of less than 4μs must follow the quasi-stable period, for the circuit to work up to 100kc/s. For this reason, the recovery-path resistor R_{33} is reduced to the minimum value permitted by the peak collector current rating of Tr_{11}, ensuring a rapid discharge of C_{17}.

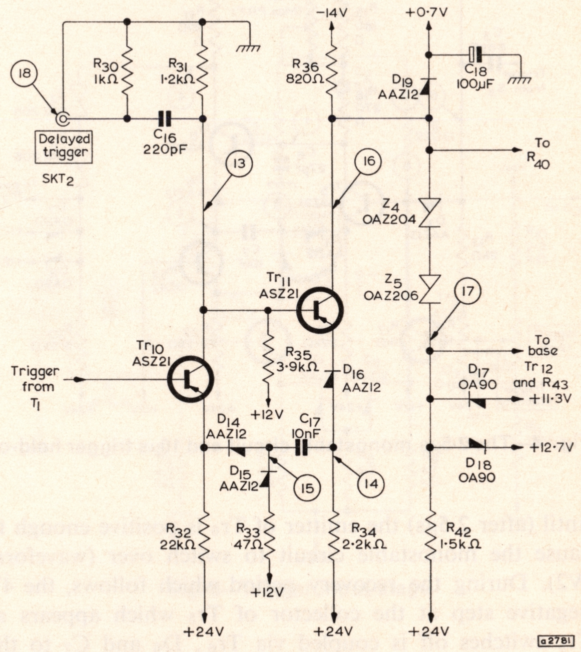
-14V
+0·7V
18
R30 1kΩ
R31 1·2kΩ
Delayed trigger
SKT2
C16 220pF
R36 820Ω
D19 AAZ12
C18 100μF
To R40
13
16
Z4 OAZ204
Z5 OAZ206
17
Tr11 ASZ21
Tr10 ASZ21
Trigger from T1
R35 3·9kΩ
D16 AAZ12
To base Tr12 and R43
D17 OA90
+11·3V
+12·7V
D18 OA90
+12V
C17 10nF
D14 AAZ12
D15 AAZ12
15
14
R32 22kΩ
R33 47Ω
R34 2·2kΩ
R42 1·5kΩ
+12V
+24V
+24V
+24V
a2781

Fig. 7—The 6μs monostable circuit

The socket SKT_2 enables positive trigger pulses of amplitude > 1V and having a p.r.f. ⩽ 100kc/s to be applied directly to this monostable circuit, thus by-passing the fixed minimum delay present in the above circuits. In this way, a minimum delay of approximately 50ns can be achieved on timebase ranges ⩽ 5ns/cm. Alternatively, the 3V positive-going pulse which appears at this socket when the monostable fires can be used to trigger an external circuit (waveform W18). In this mode, for example, the STABILITY control can be rotated fully clockwise, and the instrument becomes its own pulse generator at 100kc/s. The waveforms for this circuit are shown in W13 to W18.

Timebase Ramp Generator and Comparator Circuit

The circuits of the timebase ramp generator and comparator, shown in Fig. 8, are essentially the same as those of Tr_7 and Tr_8 described above. One major difference is the addition of Tr_{13}. This is required to discharge the largest timing capacitor (C_{19d}, providing the 0·5, 0·2 and 0·1μs/cm ranges), since the discharge current through R_{37} is insufficient to restore the ramp generator to its quiescent state within the 10μs minimum cycle-time. Tr_{13} is turned on by the overswing of voltage which appears at the collector of Tr_{11} as the monostable recovers. Its collector current is defined by R_{46} and is sufficient to discharge C_{19d} in about 2μs (waveforms W22 and W23).

Only three basic ramp durations are generated; these are 5μs, 0·5μs and 50ns (waveforms W19a to W19d). Range interpolation in a 1:2:5 sequence is achieved by scanning all, 2/5, 1/5 or 1/10 of the total ramp. The system comprising S_{e2}, R_{80}, R_{81}, R_{82} and R_{83} (Fig. 9) sets the fraction to be scanned by attenuating the staircase voltage (7·15 peak-to-peak) from the staircase generator. RV_6 sets the minimum value of the scanning voltage, and hence determines the 'get-away delay' of the timebase.

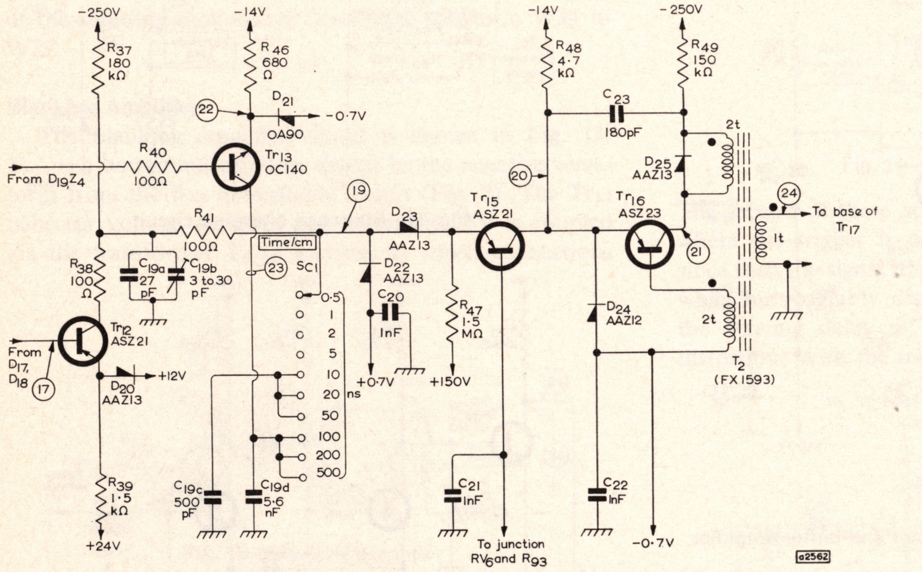
-250V
-14V
-14V
-250V
R37 180 kΩ
R46 680 Ω
R48 4·7 kΩ
R49 150 kΩ
22
D21 OA90
-0·7V
Tr13 OC140
R40 100Ω
From D19Z4
C23 180pF
20
D25 AAZ13
2t
24
To base of Tr17
1t
R41 100Ω
19
D23 AAZ13
Tr15 ASZ21
Tr16 ASZ23
21
Time/cm
SC1
23
R38 100 Ω
C19a 27 pF
C19b 3 to 30 pF
D22 AAZ13
C20 1nF
R47 1·5 MΩ
D24 AAZ12
2t
T2 (FX1593)
Tr12 ASZ21
From D17, D18 17
D20 AAZ13
+12V
0·5
1
2
5
10
20
50
100
200
500
ns
+0·7V
+150V
R39 1·5 kΩ
C19c 500 pF
C19d 5·6 nF
C21 1nF
C22 1nF
To junction RV6 and R93
-0·7V
+24V
a2562

Fig. 8—Timebase ramp generator, comparator and regenerator. The output of T_2 also connects to the signal circuit

S_E has been included to permit the use of either a 10cm or 7cm calibrated graticule on the display c.r.t. In the 7cm position, the resistor R_{84} scales down every timebase range by a factor 0·7, so that each centimetre division may be made to correspond to the time marked on the TIME/CM control even though a display of reduced size is used. By suitable choice of R_{84}, any graticule length less than 10cm can be catered for.

Regenerator Circuit

The output regenerator, Tr_{16}, also shown in Fig. 8, is similar to the regenerator described above, and serves the same purpose, namely, to provide a standard output trigger pulse to drive the following circuits. A larger feedback capacitor (C_{23}) is used, to provide a pulse of sufficient amplitude into a 100Ω line. This, and the fact that the available recharge time may be only 4μs, necessitates an increased value of discharge current, and this is ensured by reducing the collector resistor R_{49} to 150kΩ.

The waveforms from this circuit are shown in W20, W21 and W24, the latter showing a single output pulse. The amplitude of the output pulse is constant within ±1% over the whole of the timebase range.

0·5μs Monostable and Buffer Stages

A 0·5μs pulse is required at each sample-time for the following purposes:

(i) To step up the staircase generator
(ii) To operate the 'reference charge' generators (Refs. 1 and 3)
(iii) To gate on the amplifiers in the signal circuits (Refs. 1 and 3)

The circuit is shown in Fig. 10.

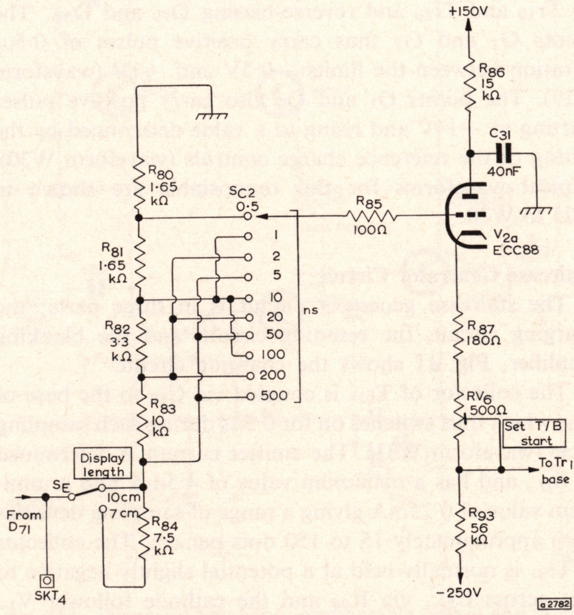
+150V
R86 15 kΩ
C31 40nF
R80 1·65 kΩ
SC2 0·5
R85 100Ω
V2a ECC88
R81 1·65 kΩ
1
2
5
10
20
50
100
200
500
ns
R82 3·3 kΩ
R87 180Ω
RV6 500Ω
R83 10 kΩ
Set T/B start
To Tr15 base
Display length
SE
10cm
7cm
From D71
R84 7·5 kΩ
R93 56 kΩ
SKT4
-250V
a2780

Fig. 9—Range interpolator and buffer amplifier

Tr$_{17}$ and Tr$_{18}$ form an emitter-timed monostable circuit producing a 0·5µs pulse on receipt of a trigger from T$_2$. In the quiescent state D$_{29}$ and D$_{30}$ are forward biased, because of the currents through R$_{55}$ and R$_{58}$. Points G$_1$ and G$_2$ are, therefore, caught at −0·5V while Tr$_{19}$ and Tr$_{20}$ are cut off, and their collectors are at −14V. During the monostable period, the collector current of Tr$_{17}$ (approximately 10mA) divides in R$_{56}$ and R$_{57}$, turning on Tr$_{19}$ and Tr$_{20}$ and reverse-biasing D$_{29}$ and D$_{30}$. The points G$_1$ and G$_2$ thus carry positive pulses of 0·5µs duration between the limits −0·5V and +1V (waveform W29). The points Q$_1$ and Q$_2$ also carry positive pulses starting at −14V and rising to a value determined by the setting of the reference charge controls (waveform W30). Typical waveforms for this monostable are shown in W25 to W28.

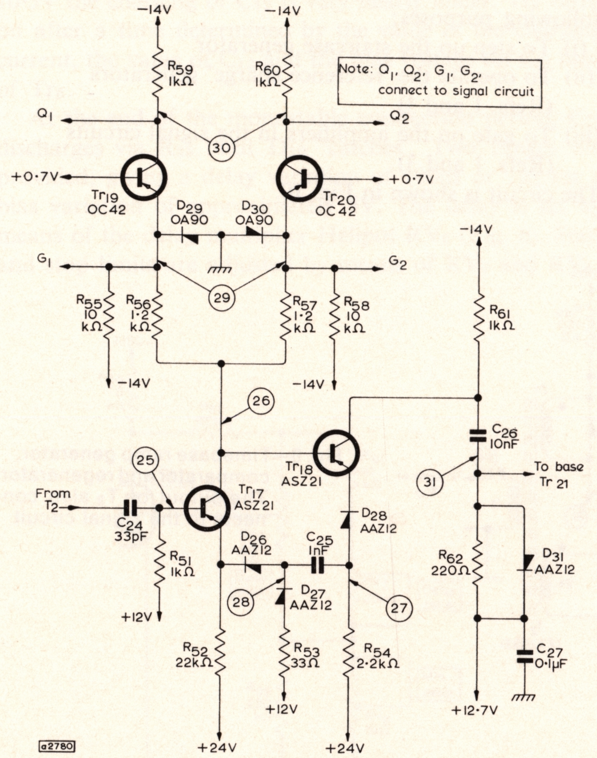
−14V
−14V
R59 1kΩ
R60 1kΩ
Note: Q1, Q2, G1, G2, connect to signal circuit
Q1
Q2
30
+0·7V
+0·7V
Tr19 OC42
Tr20 OC42
D29 OA90
D30 OA90
G1
G2
29
R55 10 kΩ
R56 1·2 kΩ
R57 1·2 kΩ
R58 10 kΩ
−14V
−14V
−14V
R61 1kΩ
26
C26 10nF
25
31
To base Tr 21
Tr18 ASZ21
From T2
C24 33pF
Tr17 ASZ21
D28 AAZ12
D26 AAZ12
C25 1nF
R51 1kΩ
28
D27 AAZ12
27
R62 220Ω
D31 AAZ12
+12V
R52 22kΩ
R53 33Ω
R54 2·2kΩ
C27 0·1µF
+12V
+12·7V
+24V
+24V
a2780

Fig. 10—The 0·5µs monostable circuit and buffer amplifier

Staircase Generator Circuit

The staircase generator circuit is in three parts; the charging circuit, the resetting circuit, and the blanking amplifier. Fig. 11 shows the charging circuit.

The collector of Tr$_{18}$ is coupled via C$_{26}$ to the base of Tr$_{21}$ which thus switches on for 0·5µs during each sampling cycle (waveform W31). The emitter current is determined by S$_D$, and has a maximum value of 4·5mA and a minimum value of 0·25mA giving a range of sampling densities from approximately 15 to 150 dots per cm. The collector of Tr$_{21}$ is normally held at a potential slightly negative to that across C$_{28}$, via R$_{66}$ and the cathode follower V$_1$. The diode D$_{34}$ is, thus, reverse-biased. When Tr$_{21}$ is switched on, D$_{34}$ conducts, and a short pulse (waveform W32) is injected into C$_{28}$ which charges up through one step.

The charge on C$_{28}$ decays slowly during the inter-trigger periods, because of leakage currents; these are minimised by using silicon diodes. A cathode-follower is essential here as an output buffer. The maximum period between steps can be extended to over 1s before the droop on each step becomes excessive. The minimum period is determined to some extent by the hole-storage in D$_{34}$, and therefore a low minority carrier storage diode type SX781 is used. The linearity of the generated waveform is very good, as shown in waveform W33, and the linearity error can be calculated using the expressions derived in Appendix 2.

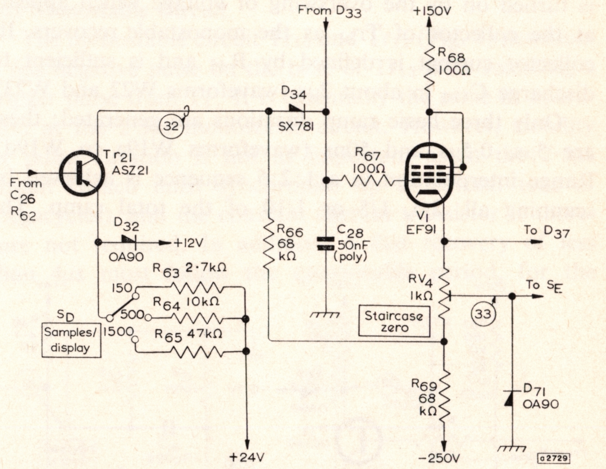
From D33
+150V
R68 100Ω
D34 SX781
32
Tr21 ASZ21
From C26 R62
R67 100Ω
V1 EF91
D32 OA90
+12V
R66 68 kΩ
C28 50nF (poly)
To D37
R63 2·7kΩ
150
R64 10kΩ
500
SD Samples/ display
1500
R65 47kΩ
RV4 1kΩ
Staircase zero
To SE
33
R69 68 kΩ
D71 OA90
+24V
−250V
a2729

Fig. 11—Staircase charging circuit

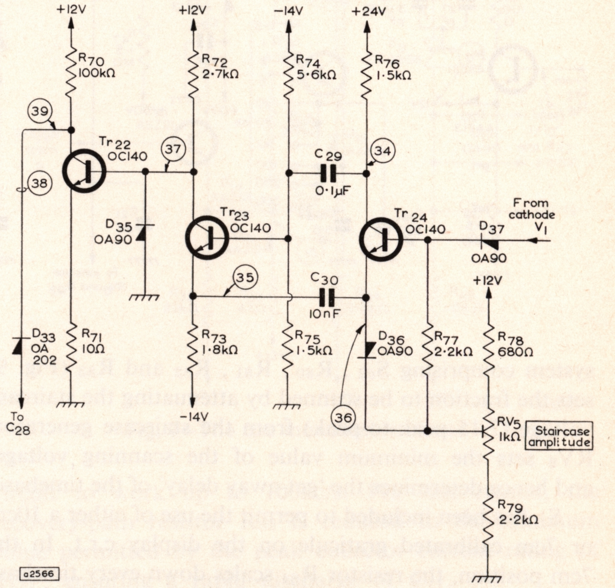
+12V
+12V
−14V
+24V
R70 100kΩ
R72 2·7kΩ
R74 5·6kΩ
R76 1·5kΩ
39
Tr22 OC140
37
C29 0·1µF
34
38
D35 OA90
Tr23 OC140
Tr 24 OC140
From cathode V1
D37 OA90
35
C30 10nF
+12V
D33 OA 202
R71 10Ω
R73 1·8kΩ
R75 1·5kΩ
D36 OA90
R77 2·2kΩ
R78 680Ω
To C28
−14V
36
RV5 1kΩ
Staircase amplitude
R79 2·2kΩ
a2566

Fig. 12—Staircase reset monostable circuit

D$_{71}$ is included to prevent a lock-out around the system Tr$_{15}$, Tr$_{16}$, Tr$_{17}$, Tr$_{21}$ and V1; such a lock-out can cause a long delay, subsequent to the equipment being switched on, before the staircase generator can operate. The probable sequence of events which lead to a lock-out in the absence of D$_{71}$ is as follows. During the warm-up period, the grid current of V$_1$ charges C$_{28}$ to a negative potential. When this period is over, the cathode of V$_1$ remains fairly negative, so that the comparator is always cut off. No trigger pulses reach the pump monostable circuit, so that the charge on C$_{28}$ must be allowed to leak away before the loop can become active. If the leakage currents are unfavourable, a stable lock-out state can result.

The resetting circuit is shown in Fig. 12. After the selected number of steps have been generated, D$_{37}$ conducts and triggers the emitter-timed monostable Tr$_{23}$ and Tr$_{24}$. The precise trigger level (and hence the staircase amplitude) is set by RV$_5$. The 5µs positive pulse at the collector of Tr$_{23}$ turns off Tr$_{22}$, which discharges C$_{28}$ via D$_{33}$. The whole resetting operation always takes place before Tr$_{21}$ produces the next pulse. The waveforms of the resetting monostable circuit are shown in W34 to W39.

Blanking Amplifier

The blanking amplifier circuit is shown in Fig. 13. Tr$_{14}$ is a bottoming amplifier driven by the negative waveform from the 6µs monostable circuit (Fig. 7). The Tr$_{14}$ collector voltage swing of approximately 25V is coupled via the transformer T$_6$ to sockets, to which connections to the grid or cathode of the display c.r.t. can be made, to provide blanking of the display. This suppresses some short transients which unavoidably appear on the y-deflection voltage during each sampling period, and tend to cause an apparent thickening of the trace, especially at the highest y-sensitivity settings, and at high p.r.f.

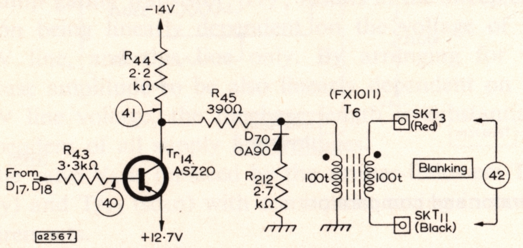
−14V
R44 2·2 kΩ
41
R45 390Ω
(FX1011) T6
SKT3 (Red)
D70 OA90
R43 3·3kΩ
From D17, D18
Tr14 ASZ20
R212 2·7 kΩ
100t
100t
Blanking
42
40
SKT11 (Black)
a2567
+12·7V

Fig. 13—Blanking amplifier

The waveforms of this circuit are shown in W40 to W42. Note that the heavy bottoming of Tr$_{14}$ causes stretching of the voltage pulse to about 8µs.

POSSIBLE MODIFICATIONS

Since the above circuits were designed (mid-1961), several improvements or alternative arrangements have become apparent. These modifications result in improved performance and greater simplicity or both. Some of the supply rails are also unnecessary.

Delay Circuit

A separate ramp generator for the delaying function was originally used, since this permits the trigger delay to be independent of the timebase range. However, it is questionable whether this is advantageous. An alternative method is to use a single ramp for both trigger delay and timebase purposes, as shown in Fig. 14. This permits a delay variation of (say) ten times the basic 'TIME/CM' value. A single ramp system is now the preferred arrangement in most commercial instruments. One manufacturer has modified the timing unit in this way to offer better delaying facilities (for example see Ref. 4.)

The advantages of such a method are that since none of the components used in the delay circuits (above) are required, a more economical system is achieved while at the same time a lower value of minimum delay is obtained.

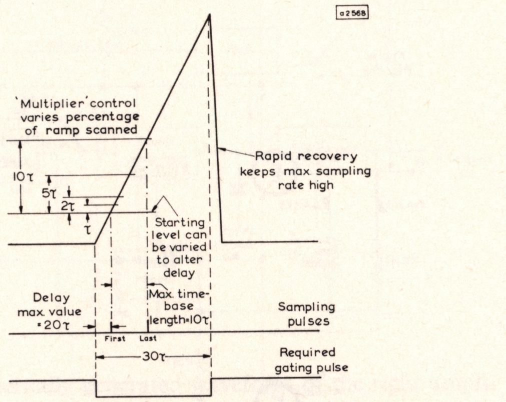
a2568
'Multiplier' control varies percentage of ramp scanned
10τ
5τ
2τ
τ
Rapid recovery keeps max. sampling rate high
Starting level can be varied to alter delay
Delay max. value =20τ
Max. time-base length=10τ
Sampling pulses
First
Last
30τ
Required gating pulse

Fig. 14—Single ramp system

The second of these advantages is particularly important where the trigger is derived from the signal waveform, since then the signal must be passed through a delay cable, which unavoidably distorts the pulse shape. The longer the starting delay in the timebase, the greater is this distortion. With the method suggested, a minimum delay

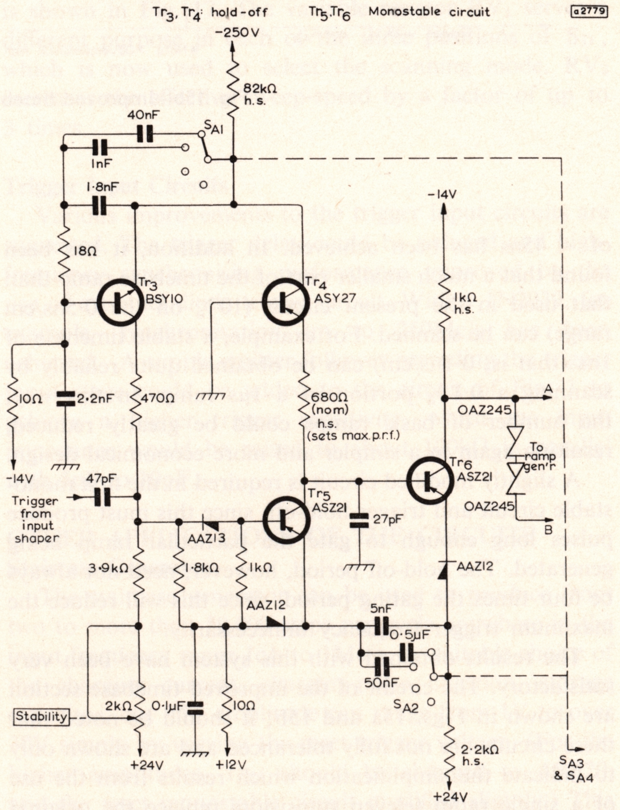
Tr3, Tr4: hold-off
Tr5, Tr6 Monostable circuit
a2779
−250V
82kΩ h.s.
40nF
SA1
1nF
1·8nF
−14V
18Ω
Tr3 BSY10
Tr4 ASY27
1kΩ h.s.
10Ω
2·2nF
470Ω
680Ω (nom) h.s. (sets max.p.r.f.)
A
OAZ245
To ramp gen'r
−14V
47pF
Trigger from input shaper
Tr6 ASZ21
Tr5 ASZ21
27pF
OAZ245
B
AAZ13
3·9kΩ
1·8kΩ
1kΩ
AAZ12
AAZ12
5nF
0·5µF
50nF
SA2
Stability
2kΩ
0·1µF
10Ω
+24V
+12V
2·2kΩ h.s.
+24V
SA3 & SA4

Fig. 15a—Improved timebase: monostable circuit and hold-off circuit

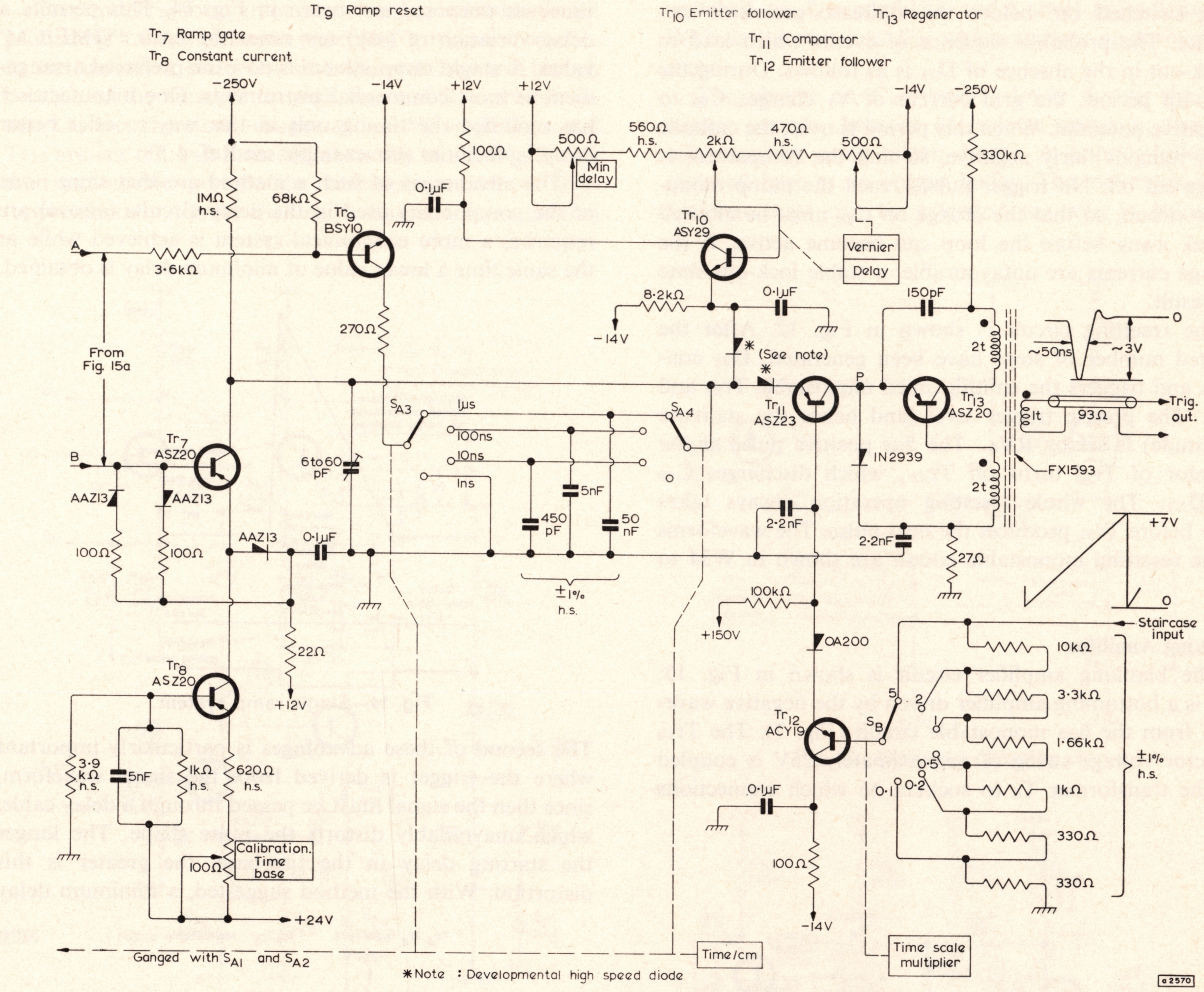
Tr9 Ramp reset
Tr7 Ramp gate
Tr8 Constant current
Tr10 Emitter follower
Tr11 Comparator
Tr12 Emitter follower
Tr13 Regenerator
−250V
−14V
+12V
+12V
−14V
−250V
500Ω h.s.
560Ω h.s.
2kΩ
470Ω h.s.
500Ω
100Ω
Min delay
330kΩ
1MΩ h.s.
68kΩ
0·1μF
Tr9 BSY10
Tr10 ASY29
Vernier
Delay
A
3·6kΩ
8·2kΩ
−14V
0·1μF
150pF
270Ω
(See note)
~50ns
~3V
2t
From Fig. 15a
P
Tr11 ASZ23
Tr13 ASZ20
SA3
1μs
100ns
10ns
1ns
SA4
1t
93Ω
Trig. out.
B
Tr7 ASZ20
6 to 60 pF
5nF
1N2939
FX1593
AAZ13
AAZ13
450 pF
50 nF
2·2nF
2t
100Ω
100Ω
AAZ13
0·1μF
2·2nF
+7V
27Ω
±1% h.s.
100kΩ
+150V
OA200
Staircase input
22Ω
Tr8 ASZ20
+12V
10kΩ
3·3kΩ
Tr12 ACY19
SB
1·66kΩ
3·9kΩ h.s.
5nF
1kΩ h.s.
620Ω h.s.
0·1μF
1kΩ
0·5
0·2
0·1
330Ω
330Ω
±1% h.s.
Calibration. Time base
100Ω
100Ω
+24V
−14V
Ganged with SA1 and SA2
Time/cm
Time scale multiplier
*Note : Developmental high speed diode
e2570

Fig. 15b—Improved timebase: generator and comparator

of < 45ns has been achieved. In addition, it has been found that a much smaller part of the timebase ramp than that used in the present circuit (10% on the 0·5ns/cm range) can be scanned. For example, a stable timebase of 1ns (that is, 0·1ns/cm) can be obtained quite reliably by scanning a 0·1% portion of a 1μs ramp. In this way, the number of basic ramps could be greatly reduced, resulting again in a simpler and more economical design.

A slightly modified circuit is required in the first monostable circuit and trigger hold-off, since this must produce pulses long enough to gate the particular ramp being generated. The hold-off period, however, need not always be four times the gating period, since this will reduce the maximum trigger frequency unnecessarily.

The results obtained with this system have been very satisfactory. The circuit of the improved timebase section are shown in Figs. 15a and 15b; it should be noted that these circuits are not fully toleranced and are shown only to indicate the simplification which results from the use of a single ramp (eleven transistors replace the original fourteen transistors and two triodes).

The system performance is as follows:

BASIC TIMES/CM:	1μs, 100ns, 10ns, 1ns
SCALE MULTIPLIER:	×5, ×2, ×1, ×0·5, ×0·2, ×0·1
OVERALL RANGE:	5μs/cm to 100 ps/cm
DELAY VARIATION:	150 times basic TIME/CM value
MIN. DELAY:	< 45ns below 50ns/cm
JITTER:	< 1:10 000, or < 30ps, whichever is greater
MAX. REP. RATE:	100kc/s on 10ns and 1ns ranges 25kc/s on 100ns range 2·5kc/s on 1μs range (The scale multiplier does not affect max. rep. rate)
MAX. SYNC. FREQUENCY:	> 50Mc/s in input circuit in Fig. 3, on ranges below 10ns/cm (see below).

S$_A$ and S$_B$ could be replaced by one switch giving 15 calibrated ranges between 5μs and 100ps/cm, although there is some advantage in the extra flexibility permitted by the separate 'MULTIPLIER' control.

The avalanche generator, Tr$_{13}$, introduces a delay of up to 20ns, which is a large proportion of the overall delay. This might be reduced by replacing the regenerator by a 0·5μs blocking oscillator connected directly to point 'P', which would also generate the gating waveforms at present generated by Tr$_{17}$ to Tr$_{20}$ of Fig. 10. The diode in the collector of Tr$_{11}$ produces a 400mV step of substantially constant speed and improves the stability of output pulse amplitude against range-changes, and also reduces jitter on the slower ranges.

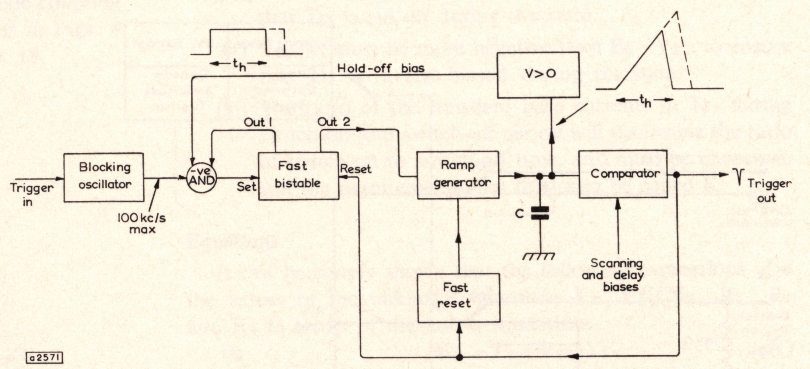
Trigger in
Blocking oscillator
100kc/s max
−ve AND
Out 1
Out 2
Set
Fast bistable
Reset
Hold-off bias
V>0
t_h
t_h
Ramp generator
Comparator
Trigger out
C
Scanning and delay biases
Fast reset
e2571

Fig. 16—Alternative system

In this circuit, several other improvements are made. The use of a constant current transistor, Tr$_8$, to supply the ramp gating transistor, Tr$_7$, results in the sweep calibration being linearly dependent on the voltage of the +24V line, and this line only. By arranging for the staircase amplitude to be also linearly dependent on the +24V line voltage, the timebase length is substantially independent of all supply line voltages.

The valve V$_2$ is replaced by the emitter-followers Tr$_{10}$ (delay) and Tr$_{12}$ (scan) with consequent saving in power requirements.

It has been found that imperfect decoupling of supply lines leads to 'base-line wriggles' on the final display when viewing at maximum sensitivity. The decoupling networks have therefore been improved.

In another possible arrangement the monostable circuit is replaced by a bistable circuit as shown in Fig. 16. Here, the hold-off period lasts just long enough for the ramp to reach the current value of the scanning bias and reset to zero, when the next trigger is applied. Higher repetition rates on longer timebase ranges could probably be achieved in this way. The trigger input blocking oscillator limits the upper frequency to 100kc/s.

C.R.T. Blanking

The transients on the transformed signal output (Ref. 3) last for 1 to 2μs after each sample. The c.r.t. trace should be blanked-out during this interval. With the present circuit, blanking starts at the beginning of the timebase and lasts for about 8μs. Thus, an unnecessarily long blanking interval is used, and some brightness variation over the scan on slow sweeps might result. A better method would be to make Tr$_{14}$ and T$_6$ (Fig. 13) into a 2μs blocking oscillator which is fired at the beginning of each sample.

Staircase Reset

A 5μs blocking oscillator could replace the present 5μs emitter-timed monostable circuit, which resets the staircase to zero, resulting in greater simplicity and perhaps lower cost.

Scanning System

In the present circuit, the scanning voltage is derived from the staircase generator. However, there is no reason why an externally generated waveform of the right amplitude and d.c. level should not be used for scanning. Alternatively, scanning can be achieved by manual rotation of a suitable control. Also, the sampling densities can be varied continuously by replacing S$_D$ (Fig. 11) by a variable resistor. Finally, a continuous variation of the effective sweep-speed can be provided by varying the division ratio to the comparator.

A modification which introduces all of these facilities is shown in Fig. 17. The variable resistor RV$_1$ serves a different purpose in each of the three positions of S$_D$, which is now used to select the scanning mode. RV$_2$ increases the effective sweep-speed by a factor of up to 3 times.

Trigger Input Circuits

Various improvements to the trigger input circuits are suggested. The trigger delay could be reduced and high-frequency synchronising performance improved by the use of a tunnel diode trigger circuit. With a 1N2939, for example, synchronisation up to 250Mc/s has been achieved. A simple emitter-follower preceding the trigger input stage could be added to the circuit of Fig. 3 to achieve a higher trigger sensitivity, whilst the trigger input impedance would be raised to about 100kΩ in parallel with 5pF to 10pF.

OTHER APPLICATIONS OF THE CIRCUITS

Staircase Generator

The staircase generator can be used to produce from two to more than 50 000 steps per cycle anywhere in the input frequency range 1c/s to 1Mc/s, by suitable choice of the charging current, charging-pulse duration, storage capacitor, etc. The amplitude can range from 1V to over 30V simply by varying the reset trigger voltage. (For the higher amplitudes, Tr$_{21}$ should be changed to ASZ20, and the reset monostable circuit modified slightly.) This wide range of operation, coupled with excellent linearity, makes the circuit suitable for many systems requiring an accurate staircase waveform.

By replacing the pump circuit Tr_{21}, D_{34} and R_{66} by a p-n-p silicon transistor arranged as a constant current generator, this circuit may be modified into a wide-range current (or voltage) controlled oscillator, producing a very linear sawtooth with a 2 to $3\mu s$ 'flyback' time over the range 0·05c/s to 50kc/s. Measurements indicate a linear current-frequency law over at least five decades, and a linear voltage-frequency law over about two decades, using a simple emitter-stabilised configuration for the constant-current generator.

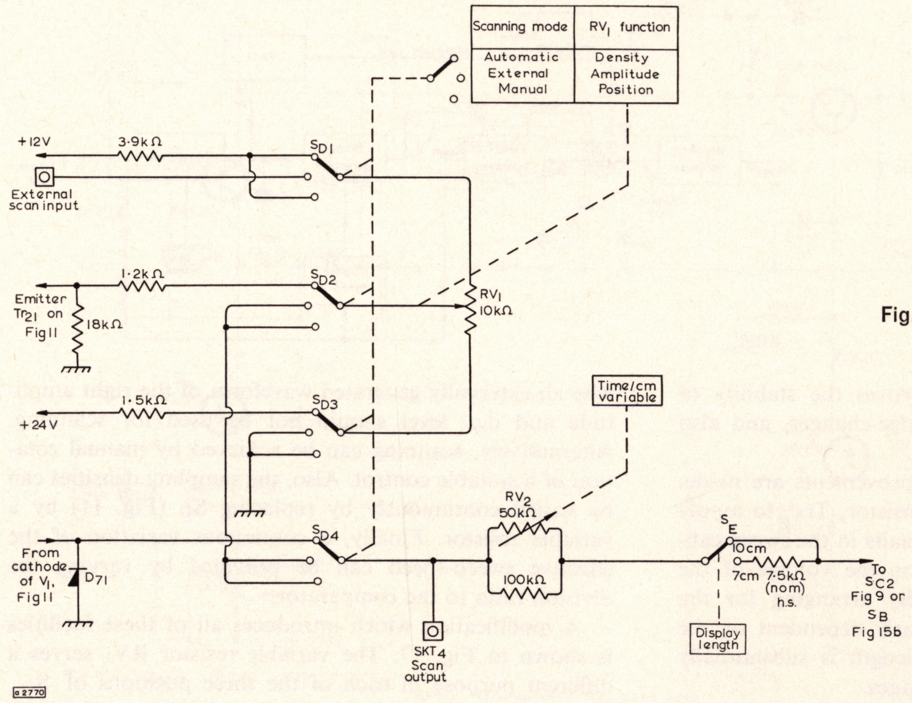

Fig. 17—Modified scanning mode control

Delay Circuit

The present delay circuit has two delay ranges giving variations of 100ns and $1\mu s$. However, these ranges can easily be extended, and full-scale delay variations from 10ns to several milliseconds can be obtained. The long recovery time of the delay ramp generator (Fig. 5) can be a disadvantage, especially on very long delay ranges, in which case the rapid recharging method of the timebase circuit (Fig. 8) might be used.

The linearity of delay as a function of comparator bias is good. (See Appendix 2, page 222.) Jitter is low, and a delay value of $< 10^{-4}$ times the range period is typical. This might be improved by increasing the ramp amplitude, so as to reduce the effects of pick-off noise.

The output trigger pulse is independent of the delay range, and is a narrow negative pulse at low impedance, the amplitude and duration of which can be adjusted by means of the feedback capacitor (C_{15} in Fig. 5).

A disadvantage of the circuit is that the calibration accuracy depends on the stability of the supply-rail voltages. An alternative arrangement is one in which any supply-rail variations cause proportional changes in the rate-of-rise of the ramp and the comparator bias as in Fig. 15b. However, in the original circuits described this dependence is not excessive, and with straightforward supply-line regulators the stated accuracy of ±2% can be maintained for mains voltage changes of ±10%.

Monostable Circuit

It is pointed out in Reference 2 that the emitter-timed monostable circuit can be used as a linear sawtooth generator. This feature, together with the high trigger sensitivity, makes the circuit very useful as a timebase circuit for a conventional oscilloscope. With a high-voltage high-speed transistor such as the ASZ20 or BSY10 (n-p-n), sawtooth waveforms of good linearity and several tens of volts amplitude can be obtained down to the microseconds region.

The addition of a trigger input stage and a trigger hold-off circuit as shown in Figs. 3 and 4 (with modified component values) provides the basis for a versatile timebase generator (Ref. 5). Long sweep times, however, are difficult to obtain in this way.

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APPENDIX 1

Current-mode Coupling Network

It is often necessary to couple two switching transistors in such a way that the most efficient use is made of the collector current of the first transistor in switching on or off the second transistor. The time taken for the second transistor to switch is dependent on the amount of transient current available to charge or discharge its base and the associated capacitances. Where d.c.-coupling is also required for a particular reason, and a voltage shift must be introduced, a zener-diode coupling network is frequently used. Examples of this occur in Figs. 4 and 7, and the generalised circuit is shown in Fig. 18.

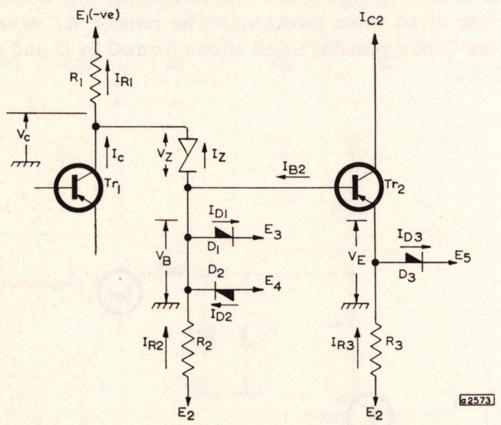

Fig. 18—Zener diode coupling networks

Tr_1 and Tr_2 are assumed to be emitter-current-switched stages, in which the collector current is independent of the collector circuit conditions, provided that the transistor does not bottom.

Definitions

The ON and OFF states are defined as follows:

ON state: Tr_2 is conducting, and its emitter current is defined by R_3. D_2 is forward biased and Tr_1 is at its lowest value of collector current (or cut off).

OFF state: Tr_2 is cut off, D_1 is forward biased, Tr_1 is at its highest value of collector current.

In addition to the symbols shown in Fig. 18, the following are defined:

V_1 = forward bias voltage across D_1 during OFF state
V_2 = forward bias voltage across D_2 during ON state
V_3 = forward bias voltage across D_3 during OFF state
V_{EB} = forward bias emitter voltage of Tr_2 during ON state
V_Z = reverse breakdown voltage of the zener diode.

These terms are current-dependent, but will be considered as constant for simplicity. In a practical calculation, the values at the anticipated current levels are used:

I_{D1} = forward current in D_1 during OFF state
I_{D2} = forward current in D_2 during ON state
I_E = required value of emitter current of Tr_2 during ON state.

The subscripts ON and OFF will be used to denote the value of a variable in a given state. Leakage currents are neglected, since they are normally small compared with the practical values of currents associated with the network.

Conditions

The following conditions must be satisfied for the network to operate correctly.

(i) $I_Z > 0$, to ensure that the zener diode is in reverse conduction at all times.

(ii) $I_{D1} > 0$ and $I_{D2} > 0$ to define catching potentials.

(iii) $V_{C(ON)}$ and $V_{C(OFF)}$ must each fall between specified limits, to ensure that the requirements for the rest of the circuit associated with Tr_1 are met.

(iv) $V_{B(OFF)}$ must be more positive than E_5+V_3, to ensure that Tr_2 is cut off during OFF state.

(v) $V_{B(ON)}$ must be more negative than E_5-V_{EB} to ensure that D_3 is reverse-biased during ON state.

(vi) The ratio of the transient base currents in Tr_2 during switch-on and switch-off period will determine the ratio of switch-on to switch-off time, and must be chosen to suit the requirements. Let this ratio be called K.

Equations

It can be simply shown that the following expressions give the values of the unknown quantities E_3, E_4, V_Z, R_1, R_2 and R_3 in terms of the known quantities.

(i)
$$E_3 > E_5+V_3-V_1 \qquad \ldots(1)$$
$$E_4 < E_5+V_2-V_{EB} \qquad \ldots(2)$$

Note These catching rails will usually be kept to the minimum value required for correct operation to reduce delay time and the time taken for the emitter current of Tr_2 to reach its final value. This is because of stray capacitances.

(ii)
$$V_Z = E_4-V_2-V_{C(ON)} \qquad \ldots(3)$$

or

$$V_Z = E_3+V_1-V_{C(OFF)} \qquad \ldots(4)$$

Note It is assumed that only $V_{C(ON)}$ or $V_{C(OFF)}$ must be specified, since in practice the voltage swing $V_{C(OFF)}-V_{C(ON)}$ is small. If it is necessary for some reason to define both $V_{C(ON)}$ and $V_{C(OFF)}$, the minimum value of E_3 required to ensure cut-off of Tr_2 during the OFF state would first be calculated from Eq(1), then V_Z from Eq(4) and finally E_4 from Eq(3).

(iii)
$$R_3 = \frac{E_2-E_4+V_2-V_{EB}}{I_E} \qquad \ldots(5)$$

(iv)
$$R_1 = \frac{V_{C(OFF)}-E_1}{I_{Z(OFF)}+I_{C(OFF)}} \qquad \ldots(6)$$

Notes (a) E_1 is a negative supply rail, and R_1 is thus positive.

(b) $I_{Z(OFF)}$ is the minimum value of zener current at which it is desired to operate, that is, at a value well in the constant-voltage region of the diode.

(v)
$$R_2 = \frac{[(V_{B(OFF)}-E_2)(1+K)-\Delta V_B]R_1}{V_B-R_1[I+(1+K)I_{Z(OFF)}]} \qquad \ldots(7)$$

where ΔV_B = voltage swing on base of T_2
$= E_3-E_4+V_1+V_2$,

$V_{B(OFF)}$ = voltage on base of Tr_2 during off state
$= E_3-V_1$,

and $I = I_{C(OFF)}-I_{C(ON)}-(1-\bar{\alpha}_2)I_E \qquad \ldots(8)$

Notes (a) $I_{C(OFF)}$ corresponds to the maximum value of the collector current of Tr_1.

(b) $\bar{\alpha}_2$ = the large signal alpha of Tr_2.

(c) This expression will only hold for K if ΔV_B is kept to the minimum value required to switch Tr_2.

Example

Suppose the known quantities to be as follows:

$V_1 = V_2 = V_3 = 0{\cdot}5\text{V}$
$V_{EB} = 0{\cdot}25\text{V}$
$V_{C(OFF)} = -3{\cdot}0\text{V}$
$E_1 = -14\text{V}$
$E_2 = +24\text{V}$
$E_5 = +12\text{V}$
$I_{Z(OFF)} = 1\text{mA}$ (minimum desired zener current)
$I_{C(ON)} = 0{\cdot}4\text{mA}$
$I_{C(OFF)} = 10\text{mA}$
$\bar{\alpha}_2 = 0{\cdot}95$ (minimum value)
$K =$ unity

From (1)

$$E_3 > +12+0{\cdot}5-0{\cdot}5$$

Put $E_3 = +12{\cdot}5\text{V}$, giving 0·5V margin

From (2)

$$E_4 < +12+0{\cdot}5-0{\cdot}25$$

Put $E_4 = 11{\cdot}75\text{V}$, giving 0·5V margin

Therefore

$$V_{B(ON)} = +11{\cdot}25\text{V}$$

and

$$V_{B(OFF)} = +13\text{V}$$

and

$$V_B = 13-11{\cdot}25 = 1{\cdot}75\text{V}$$

From (4)

$$V_Z = 12{\cdot}5+0{\cdot}5-(-3) = 16\text{V}$$

From (5)

$$R_3 = \frac{+24-11{\cdot}75+0{\cdot}5-0{\cdot}25}{12} = 1{\cdot}04\text{k}\Omega \text{ (say } 1\text{k}\Omega)$$

From (6)

$$R_1 = \frac{-3-(-14)}{1+10} = 1\text{k}\Omega$$

From (8)

$$I = 10-0{\cdot}4-(1-0{\cdot}95)12 = 9\text{mA}$$

From (7)

$$R_2 = \frac{[(13-24)(1+1)-1{\cdot}75]}{1{\cdot}75-1[9+(1+1)1]}\cdot 1 = 2{\cdot}57\text{k}\Omega$$

From these results, the values of the maximum and minimum currents in R_1 and R_2, the maximum current in the zener diode and the catching currents in D_1 and D_2 can be found:

$$I_{R1(OFF)} = \frac{(-V_Z+V_{B(OFF)}-E_1)}{R_1} = \frac{[-16+13-(-14)]}{1} = 11\text{mA}$$

$$I_{R1(ON)} = \frac{(-V_Z+V_{B(ON)}-E_1)}{R_1} = \frac{-16+11{\cdot}25-(-14)}{1} = 9{\cdot}25\text{mA}$$

$$I_{R2(OFF)} = \frac{(E_2-V_{B(OFF)})}{R_2} = \frac{24-13}{2{\cdot}57} = 4.28\text{mA}$$

$$I_{R2(ON)} = \frac{(E_2-V_{B(ON)})}{R_2} = \frac{24-11{\cdot}25}{2{\cdot}57} = 4{\cdot}97\text{mA}$$

$$I_{Z(ON)} = I_{R1(ON)}-I_{C(ON)} = 9{\cdot}25-0{\cdot}4 = 8.85\text{mA}$$

$$I_{D1} = I_{R2(OFF)}-I_{Z(OFF)} = 4{\cdot}28-1 = 3{\cdot}28\text{mA}$$

$$I_{D2} = -I_{R2(ON)}-I_{Z(ON)}+(1-\bar{\alpha}_2)I_E = -4{\cdot}97+8{\cdot}85-0{\cdot}6 = 3{\cdot}28\text{mA}$$

The last two calculations provide a check on the value of K.

It can be shown that the effect of increasing R_2 to 2·7kΩ (the nearest preferred value in the 10% range) is to increase K to 1·32, resulting in a slightly better switch-on time.

APPENDIX 2

An Examination of the Sources of Non-linearity in a Ramp Generated by a 'Constant-current Transistor' Circuit

The basic circuit is shown in Fig. 19, and practical examples occur in Figs. 5, 8 and 15b. Resistor R_1 supplies a current which holds D_2 conducting during the quiescent state and recharges C during the recovery period. (Note that in the practical circuits of Figs. 8 and 15b, recharging time is reduced by the use of an extra transistor.) The resistor R_c serves to reduce the Q of a possible tuned circuit formed by C and stray inductance, and also reduces the power dissipated in Tr_1 when E_2 is larger than the desired ramp amplitude. E_1 is a high-voltage negative supply rail (−250V in the circuits under consideration). An equivalent circuit is shown in Fig. 20 which includes all of the elements which might cause non-linearities in the generated ramp. There are two main effects which cause non-linearity. One is voltage dependent, and the other is time dependent; both are considered below.

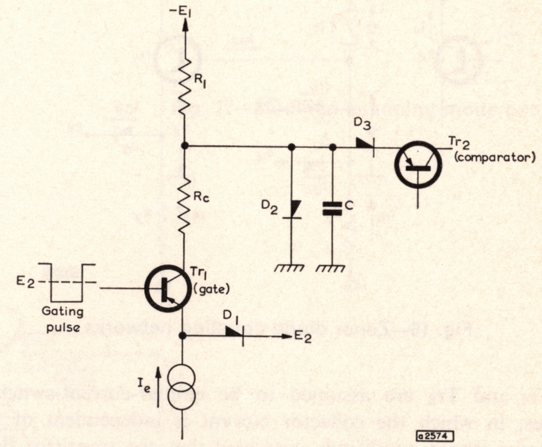

Fig. 19—Basic ramp generator

Voltage-dependent Effect

A simplified equivalent circuit is shown in Fig. 21a. This shows only those components which significantly affect the shape of the charging curve at low frequencies. R_2 represents the parallel sum of $r_{cb'}$, R_{D2} and R_{D3}. This simplifies to Fig. 21b, where E_c is the effective 'aiming potential' and R is the effective charging resistor.

E_c = steady state potential across C with $I = I_e$ (that is, $i = 0$)

$$= I_eR_2 - \frac{I_eR_2-E_1}{R_1+R_2}R_2$$

$$= \frac{R_2}{R_1+R_2}\cdot(I_eR_1+E_1) \qquad \ldots(1)$$

$$\text{and } R = \frac{R_1 . R_2}{R_1+R_2} \qquad \ldots(2)$$

Thus, the charging current for small ramp amplitudes is I_e-E_1/R_1.

During the discharging period, $I = 0$, and the steady state value of V is then E_D, where

$$E_D = E_1\cdot\frac{R_2}{R_1+R_2} \qquad \ldots(3)$$

Thus, the discharging current for small values of ramp voltages is $-E_1/R_1$ (Fig. 21c).

In practice, E_1 and I_e are fixed by other considerations. The ratio of discharging to charging-time, t_d/t_c (Fig. 21d), is also set by the available cycle-time. Let this ratio be called γ. These constants determine the value of R_1.

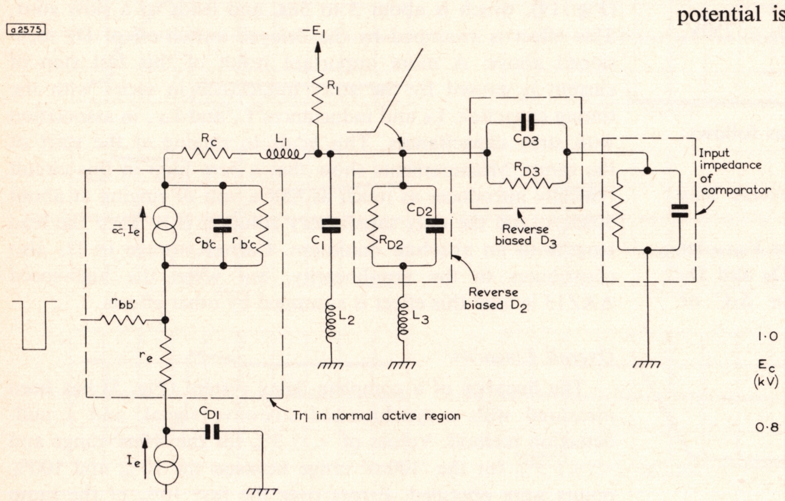

Fig. 20—Complete equivalent circuit of Fig. 19 during rise of ramp

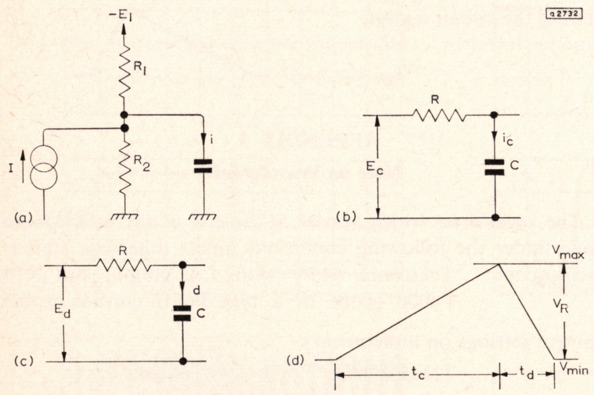

Fig. 21—Simplified circuit

We have

$$\gamma = \frac{t_d}{t_c} = \frac{i_c}{i_d} = \frac{E_c/R}{-E_D/R} = -\frac{E_c}{E_D}.$$

Substituting for E_D from Eq(3)

$$\gamma = \frac{-E_c(R_1+R_2)}{E_1R_2} \qquad \ldots(4)$$

Substituting for E_c from Eq(1)

$$\gamma E_1R_2 = \frac{-R_2}{R_1+R_2}(I_eR_1+E_1)(R_1+R_2) \qquad \ldots(5)$$

whence

$$R_1 = \frac{(1+\gamma)E_1}{I_e} \qquad \ldots(6)$$

From Eq(4)

$$E_c = \frac{\gamma E_1R_2}{R_1+R_2} = \frac{\gamma E_1R_2}{E_1(1+\gamma)-I_eR_2}. \qquad \ldots(7)$$

This is the value of the aiming potential in terms of the initial constants, and shows that there is no optimum value for I_e, but that E_c is asymptotic to $-\gamma E_1$ when $I_e \gg E_1(1+\gamma)/R_2$.

Fig. 22 is a graph showing E_c versus I_e for $R_2 = 75\text{k}\Omega$ and γ = 1, 2, 4, 7 and 10. (This value for R_2 is a minimum; values of up to 1MΩ are typical when an ASZ21 transistor and AAZ13 diodes are used.) Note that when pulsed recharging is used (as in the circuits of Figs. 8 and 15b), the effective γ becomes very large since R_1 is high, and the aiming potential is very nearly I_cR_2. For $I_e = 10\text{mA}$ and $R_2 = 75\text{k}\Omega$ this potential is 750V.

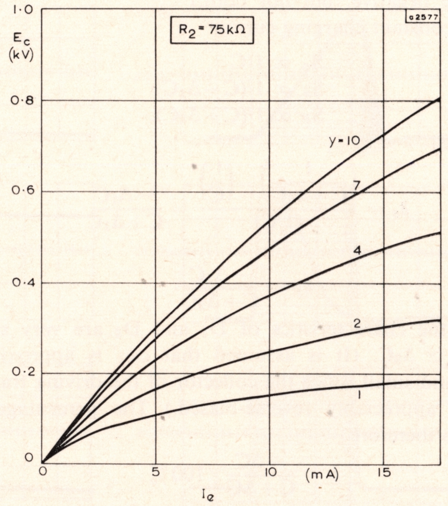

Fig. 22—Graph of effective charging potential

Non-linearity

The non-linearity error terms will be defined as

$$\delta_S = \frac{S_S-S_A}{S_A} \qquad \ldots(8)$$

and

$$\delta_F = \frac{S_F-S_A}{S_A} \qquad \ldots(9)$$

where

δ_S = error at start of ramp
δ_F = error at end of ramp
S_S = initial slope
S_F = final slope
S_A = slope at half-amplitude.

Now,

$$S_S \propto E_c-V_{MIN}$$
$$S_F \propto E_c-V_{MAX}$$
$$S_A \propto E_c-\frac{V_{MIN}+V_{MAX}}{2}.$$

Hence

$$\delta_S = \frac{E_c-V_{MIN}-E_c+\left(\dfrac{V_{MIN}+V_{MAX}}{2}\right)}{E_c-\left(\dfrac{V_{MIN}+V_{MAX}}{2}\right)} = \frac{V_R}{2E_c+V_R}$$

where

V_R = ramp amplitude.

Similarly,

$$\delta_F = \frac{-V_R}{2E_c+V_R}$$

Thus, the percentage non-linearity when $V_R \ll 2E_c$ is given by

$$\delta \simeq \pm\frac{V_R}{2E_c}\times 100\% \qquad \ldots(10)$$

In a typical case, with $V_R = 5\text{V}$, and $E_c = 750\text{V}$, $\delta = \pm 0{\cdot}3\%$.

Error Due to Voltage Sensitive Capacitances

The charging capacitance of Fig. 21 is made up as follows:

$$C = C_1 + C_{D2} + C_{D3} + C_{b'c} + \text{strays}$$

C_{D2}, C_{D3} and $c_{b'c}$ are dependent on their reverse bias voltage.

Let its value at the half-amplitude point be C; at V_{MIN} let the value be $C+\Delta_1C$ and at V_{MAX}, $C+\Delta_2C$. (If D_2 and D_3 have very different capacitances, it is possible for Δ_1C or Δ_2C to be negative, but not both.)

For a constant charging current

$$S_A \propto 1/C$$
$$S_S \propto 1/(C+\Delta_1C)$$
$$S_F \propto 1/(C+\Delta_2C).$$

From Eq(8)

$$\delta_s = \frac{\left(\frac{1}{C+\Delta_1C}\right)-\left(\frac{1}{C}\right)}{(1/C)} = \frac{-\Delta_1C}{C+\Delta_1C}.$$

Similarly

$$\delta_F = \frac{-\Delta_2C}{C+\Delta_2C}.$$

When the characteristics of D_1 and D_2 are very similar, then $\Delta_1C \simeq \Delta_2C$. (It is assumed that $c_{b'c}$ is approximately constant and small, since the collector of the driving transistor is always appreciably reverse-biased.) The percentage non-linearity is therefore

$$\delta = \frac{-\Delta C}{C+\Delta C}\times 100\%. \qquad \ldots(11)$$

ΔC will always be substantially less than the capacitance of either diode at zero reverse bias, since C_{D2} decreases as V rises, especially at low values of delay bias. It is obvious that this effect is most severe on the fastest timebases, where C is small. For example, with C = 50pF and ΔC = 2·5pF (the worst case)

$$\delta \simeq \frac{2{\cdot}5}{50}\times 100 = 5\%.$$

Another component of the voltage-dependent effect occurs at the start of the ramp and is caused because D_2 does not fully become reverse-biased until the ramp has risen by 300 to 400mV, although the current in D_2 becomes negligible after a rise of about 100mV. This effect is avoided by setting the minimum pick-off voltage above this region, but at the expense of minimum delay.

Time-dependent Effects

Time-dependent effects result in non-linearity at the beginning of the ramp, and have a duration which is mainly independent of the range capacitor, and thus are more important on the fast ranges since the effects extend further into the main portion of the ramp.

The first effect is due to the finite switch-on time of Tr_1 (Fig. 19), which is about 3 to 5ns, and leads to a slow start. This effect is swamped by the delayed switch-off of D_2 mentioned above. A more important result of this fast step of current is caused by the stray inductance in series with the timing capacitor, L_2 and inductances L_1 and L_3, in association with stray capacitances. This leads to ringing at the start of the ramp. Measurements show that a 5cm loop in this circuit typically introduces as much as half a volt of ringing at about 50Mc/s, and the only satisfactory solution is to keep the lead lengths to an absolute minimum. Carrier storage in D_2 also contributes to the non-linearity, but when the high-speed AAZ13 is used this effect is swamped by other effects.

Overall Linearity

The linearity of a complete delay system (Fig. 5) has been measured with a synchronised sinewave signal, and a null-detection method. Values of $< \pm 3\%$ for the '10ns' range and $< \pm 1{\cdot}5\%$ for the '100ns' range between the 10% and 100% points were obtained. Errors over the first 10% of the ramp were somewhat greater, but could probably be improved by altering the circuit layout.

APPENDIX 3

Note on Waveforms

The waveforms which appear at the end of the article were made under the following conditions unless otherwise stated:

Oscilloscope: Tektronix 545A with CA plug-in and X10 P6000 probe or a type P6016 current probe.

Control settings on attachment:

TIME/CM : 0·5µs/cm
DOTS : 150
DELAY : 1µs
MULTIPLIER : 0·8
DISPLAY LENGTH: 10cm
(All other controls set to give stable triggering)

Trigger rate: 25kc/s

The waveforms are numbered 1 to 42. On the circuit diagrams, voltage waveforms and current waveforms are indicated, at the point at which measurements were made by a number corresponding to one of the numbered waveforms.

WAVEFORMS ARE SHOWN ON PAGES 225 AND 226.

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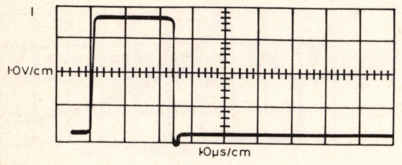

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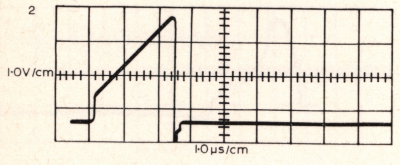

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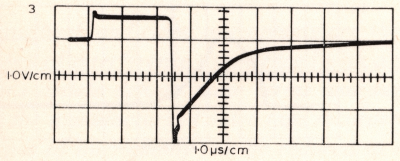

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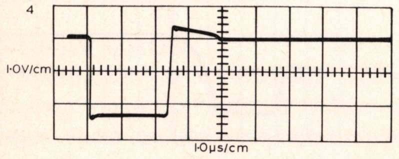

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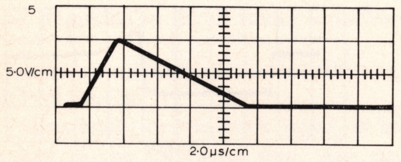

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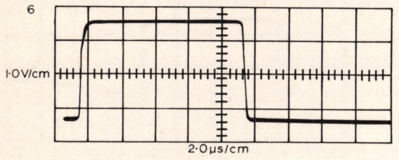

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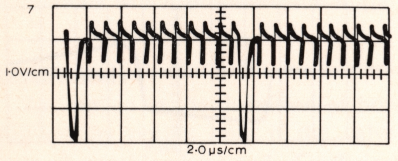

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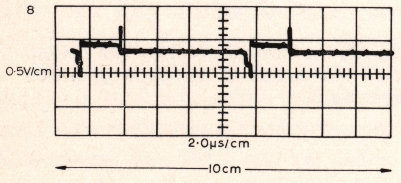

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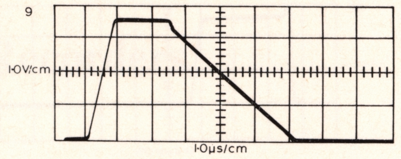

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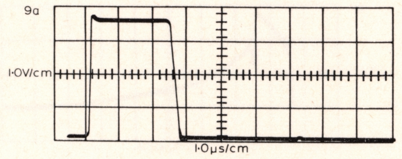

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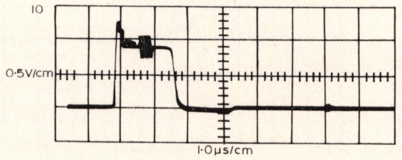

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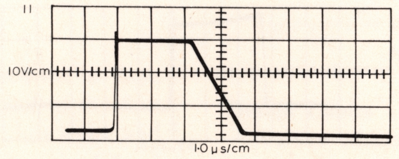

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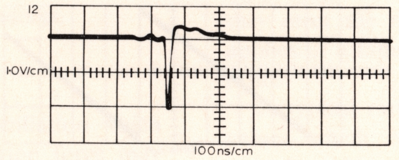

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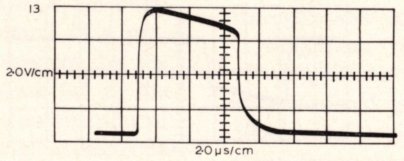

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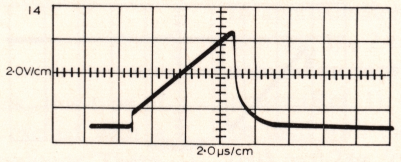

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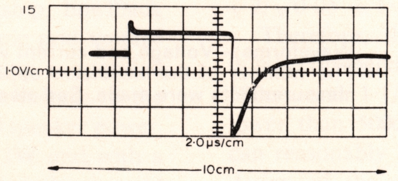

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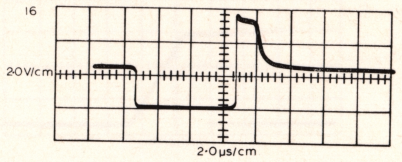

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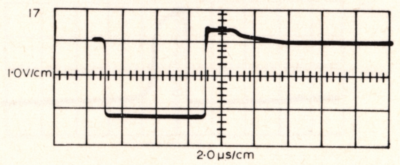

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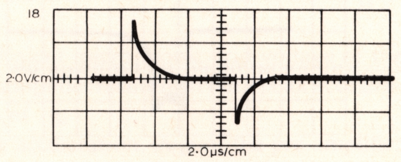

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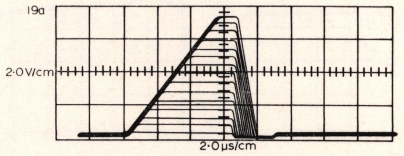

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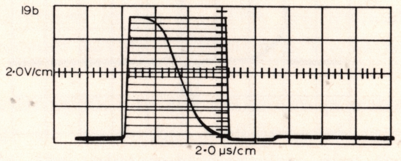

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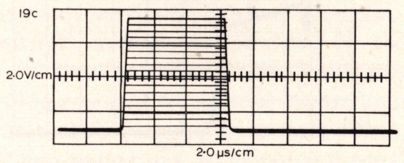

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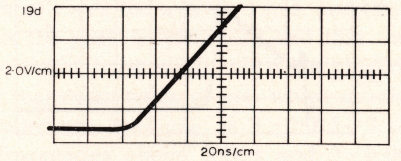

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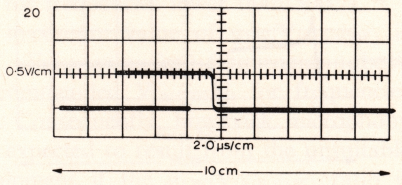

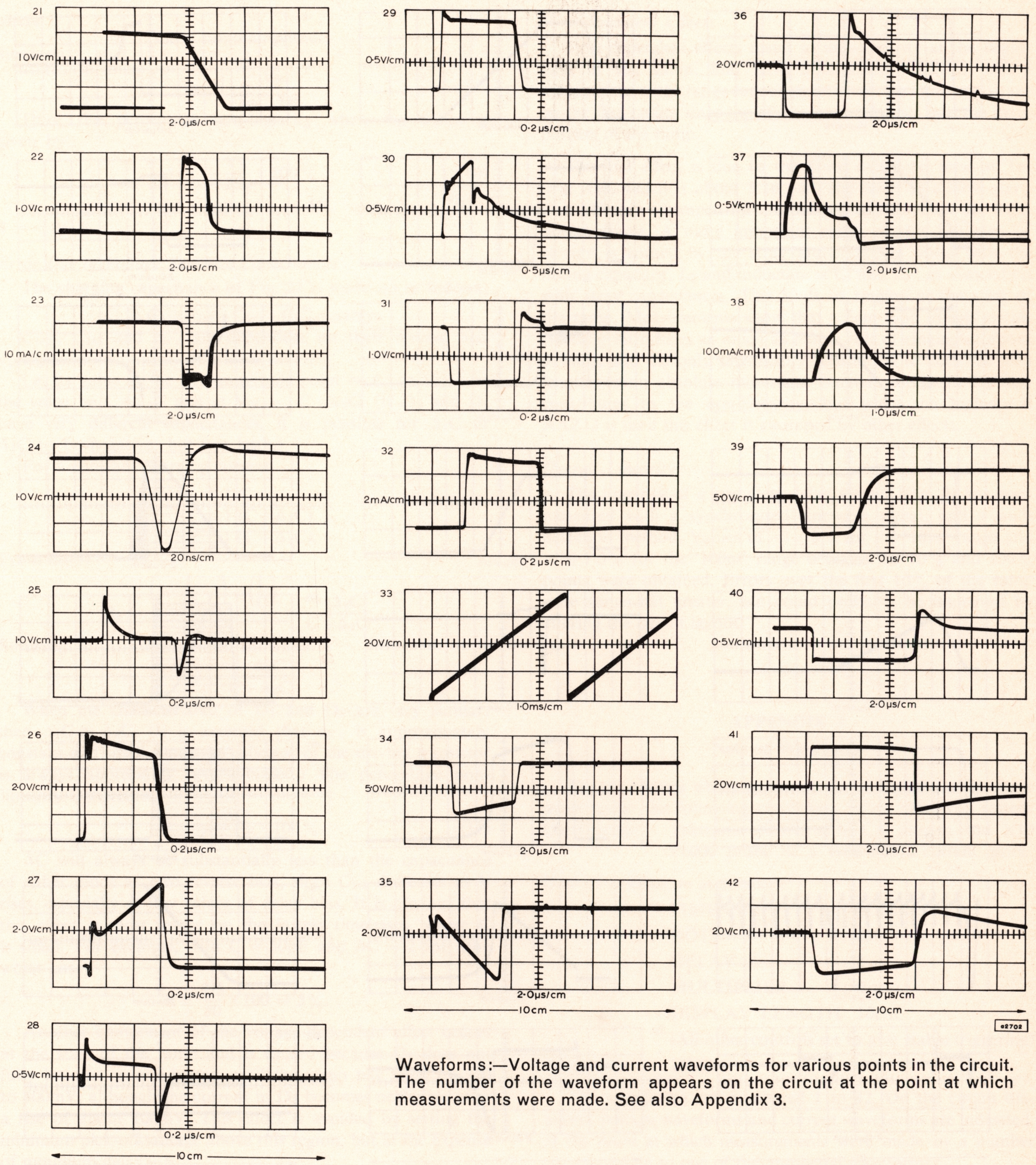

Waveforms:—Voltage and current waveforms for various points in the circuit. The number of the waveform appears on the circuit at the point at which measurements were made. See also Appendix 3.

Microphony in Tape Recorders

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Howlback and clang microphony are the two most common types of interference experienced with a valve tape recorder. This article defines these terms and suggests design limits in the manufacture of valve tape recorders whereby these two types of microphony can be reduced to a satisfactory level.

INTRODUCTION

Microphony is occasionally experienced in a tape recorder where high gain a.f. valves are used in the first stages. There are two types of microphony: howlback and clang microphony. The two types of interference are defined and discussed in detail under separate headings.

HOWLBACK

Howlback, or feedback howl, is an oscillation which occurs in the following way. Any excitation force may cause electrode vibrations in a valve resulting in an initial microphony (Ref. 1). The initial microphony of a pre-amplifier valve is then amplified and converted by the speaker into vibrations. These vibrations are fed to the valve acoustically, mechanically, or by a combination of both, in such a manner as to sustain the original electrode oscillations which produced the initial microphony.

Requirements

As implied in the definition of howlback, this type of microphony occurs only if the valve is excited with a force of suitable phase and of sufficient amplitude. Therefore, even with a suitable phase relationship, howlback will not occur if the equivalent microphonic grid voltage of the pre-amplifier valve (resulting from a specified speaker power) is less than the signal input voltage to the same valve required to produce the specified speaker power. This means that, for a speaker power of 1W and with a safety factor of two, the equivalent microphonic grid voltage $V_{eq(1W)}$ resulting from a speaker power of 1W, should be less than half the signal input voltage $V_{in(1W)}$ required for a speaker power of 1W. That is,

$$V_{eq(1W)} \leqslant \tfrac{1}{2}V_{in(1W)}$$

or, since $V_{eq(1W)} = V_{eq(1g)}\, g_{1W}$ and the speaker power is proportional to the square of the output or input voltage (or the input voltage is proportional to the square root of the speaker power),

$$V_{eq(1g)}.g_{1W} \leqslant \tfrac{1}{2}V_{in(0{\cdot}05W)}/\sqrt{0{\cdot}05}\,,$$

or

$$V_{eq(1g)}.g_{1W}/V_{in(0{\cdot}05W)} \leqslant 2{\cdot}2 \qquad \ldots(1)$$

where

$V_{eq(1g)}$ = equivalent microphonic grid voltage of the pre-amplifier resulting from a peak acceleration of 1g,

g_{1W} = peak acceleration, in g, of the pre-amplifier valve resulting from a speaker power of 1W,

$V_{in(0{\cdot}05W)}$ = signal input to the pre-amplifier valve required for a speaker power of 0·05W.

Design Limits

Valves which are intended for use in tape recorder input stages are designed with a $V_{eq(1g)}$ value such that they meet the requirement in Eq (1). This requirement applies in a tape recorder having a typical $g_{1W}/V_{in(0{\cdot}05W)}$ ratio.

A typical ratio corresponds to the maximum possible values which occur in reasonably well-designed tape recorders. Normally, the valve published data give the recommended or minimum permissible value of $V_{in(0{\cdot}05W)}$.

Maximum permissible average acceleration of the valve resulting from a speaker excitation of 50mW can be considered as 0·015g r.m.s. at frequencies higher than 500c/s, and 0·06g r.m.s. at frequencies lower than 500c/s. Considering that the maximum r.m.s. acceleration is equal to approximately three times the average r.m.s. acceleration (or $1/\sqrt{2}$ times the peak acceleration) and that the acceleration is proportional to the square root of the speaker power (Ref. 1), the maximum value of g_{1W} which should be used with the minimum $V_{in(0{\cdot}05W)}$ is $3\times0{\cdot}015\sqrt{2}/\sqrt{0{\cdot}05} = 0{\cdot}28$g for frequencies above 500c/s and $3\times0{\cdot}06\sqrt{2}/\sqrt{0{\cdot}05} = 1{\cdot}1$g for frequencies lower than 500c/s.

Therefore, the maximum value of $g_{1W}/V_{in(0{\cdot}05W)}$ is 0·28/recommended $V_{in(0{\cdot}05W)}$ for frequencies above 500c/s and 1·1/recommended $V_{in(0{\cdot}05W)}$ for frequencies lower than 500c/s. Consequently, howlback microphony can reasonably be expected to result from the unsuitable design of the equipment if the $g_{1W}/V_{in(0{\cdot}05W)}$ ratio is greater than the above-mentioned values.

CLANG

Clang is an audible interference caused by any external forces such as speaker, motors or especially switch excitations.

General Considerations

Clang may exist even at very low values of acceleration and low electrical sensitivities, although it is not necessarily objectionable at these levels. Thus, in an amplifier incorporating a speaker, if the gain is progressively increased, clang resulting from speaker excitation will be noticed first. Then, if the gain is further increased, up to a certain limit, howlback will occur.

In principle, the relative value of the interference with respect to the useful signal level determines whether the interference is negligible or not. With motor or switch excitation, the useful signal can be zero for a given interference. Therefore, ideally, the quality of motors, switches, and their mountings in the equipment should be such that the interference resulting from the excitation of these sources, with a useful signal level of zero, is not objectionable.

Generally, the clang resulting from switch excitation is more objectionable than that resulting from speaker or motor excitation. Therefore, switch excitation clang is discussed in detail and some practical requirements given.

Switch Excitation

It is important to distinguish between clang and mechanical interference. Clang is the electronic interference which is produced in the pre-amplifier valve and, after being amplified by the following stages, is audible from the loudspeaker. Mechanical interference is the sound of the switch operation as heard directly by the ear.

In the playback position the requirements for clang can be derived as follows. If the duration of the clang t_c is less than the duration of the mechanical interference t_m, the equivalent microphonic grid voltage $V_{eq(SW)}$, due to switch excitation, should be less than the signal input voltage $V_{in(P)}$ required for a speaker power of P watts, where P is the speaker output which has the same interference effect on the ear as that of the mechanical interference. That is,

$V_{eq(SW)} \leqslant V_{in(P)}$, or since $V_{eq(SW)} = V_{eq(1g)}\, g_{SW}$ and the input voltage is proportional to the square root of the speaker power,

$$V_{eq(1g)} g_{SW} \leqslant V_{in(0 \cdot 05W)} \sqrt{\frac{P}{0 \cdot 05}},$$

$$V_{eq(1g)} g_{SW} / V_{in(0 \cdot 05W)} \sqrt{P} \leqslant 4 \cdot 5 \qquad \ldots(2)$$

where g_{SW} = peak acceleration in g of the pre-amplifier valve resulting from the switching action.

If the duration of the clang is longer than that of the mechanical interference, experiment indicates that the ratio of the signal input voltage required for the maximum available speaker power $V_{in(Po)max}$ to the equivalent microphonic grid voltage $V_{eq(SW)}$ should be greater than 24dB (16 times). That is,

$$V_{eq(SW)} / V_{in(Po)max} < 1/16$$

or

$$\frac{V_{eq(1g)} . g_{SW}}{V_{in(0 \cdot 05W)} \sqrt{\frac{P_o max}{0 \cdot 05}}} < 1/16$$

or

$$V_{eq(1g)} . g_{SW} / V_{in(0 \cdot 05W)} \sqrt{P_{o(max)}} < 0 \cdot 3 \qquad \ldots(3)$$

Poor mechanical design of the equipment can produce a ringing effect and make the duration of the clang longer than that of the mechanical interference. Therefore, the problem of ringing effects should be taken into account at the design stage of the tape recorder. Thus the duration of clang would not exceed the duration of the mechanical interference and consequently, the rather rigid requirements of Eq (3) need not be considered.

Design limits for clang microphony can be derived simply, as discussed in the results given for howlback by using Eq (2) and (3) with the following typical values.

PERFORMANCE OF THREE TYPICAL TAPE RECORDERS

Measurements have been made on three different types of commercially available tape recorder.

Vibration

The acceleration of the pre-amplifier valve resulting from a speaker power of 50mW was measured, in three mutually perpendicular directions, by a Brüel and Kjaer accelerameter, type 4329, mounted on the valve socket. The peak accelerations caused by a 0·05W speaker power in the frequency spectra above 500 and below 500c/s were less than 0·05 and 0·15g respectively. The peak accelerations g_{1W} corresponding to a speaker power of 1W in the same frequency spectra were less than 0·2 and 0·7g respectively. The peak-to-peak acceleration (that is $2g_{SW}$) resulting from the operation of switches was between 0·5 and 2g, with durations of 15 to 60ms and frequencies up to 500c/s.

Electrical Sensitivity

In the playback position, the value of the input voltage $V_{in(0 \cdot 05W)}$, in the frequency range 50 to 10 000c/s, varied with frequency and the individual equipment from 0·1 to 0·8mV. The maximum available speaker power $P_{o(max)}$ varied between 1 and 3W.

Howlback, Clang and Mechanical Interference

Howlback and clang tests were carried out on the playback position with the volume control at maximum. No interference could be detected by ear.

Mechanical interference and clang resulting from switch operations were measured with a Peekel Sound Spectrometer, type GR3, and an oscilloscope. The two sources of interference were isolated with a sound-proof box, and the following results obtained:

Duration of mechanical interference t_m = 50 to 200ms.
Duration of clang t_c = 20 to 30ms.
The relative amplitude of clang with respect to the amplitude of the mechanical interference, as sensed by the spectrometer = 0·2 to 0·7.
The speaker power required to produce the same interference effect on the spectrometer as that of the mechanical interference of the switching action = 0·9 to 2·5W.

Thus, in the three tape recorders examined, it was found that clang and howlback microphony were within the limits given in this article.

REFERENCES

1. DAGPUNAR, S. S. 'Valve Microphony'. **Mullard Technical Communications,** Vol. 7, No. 61, Nov. 1962, pp. 2 to 17.